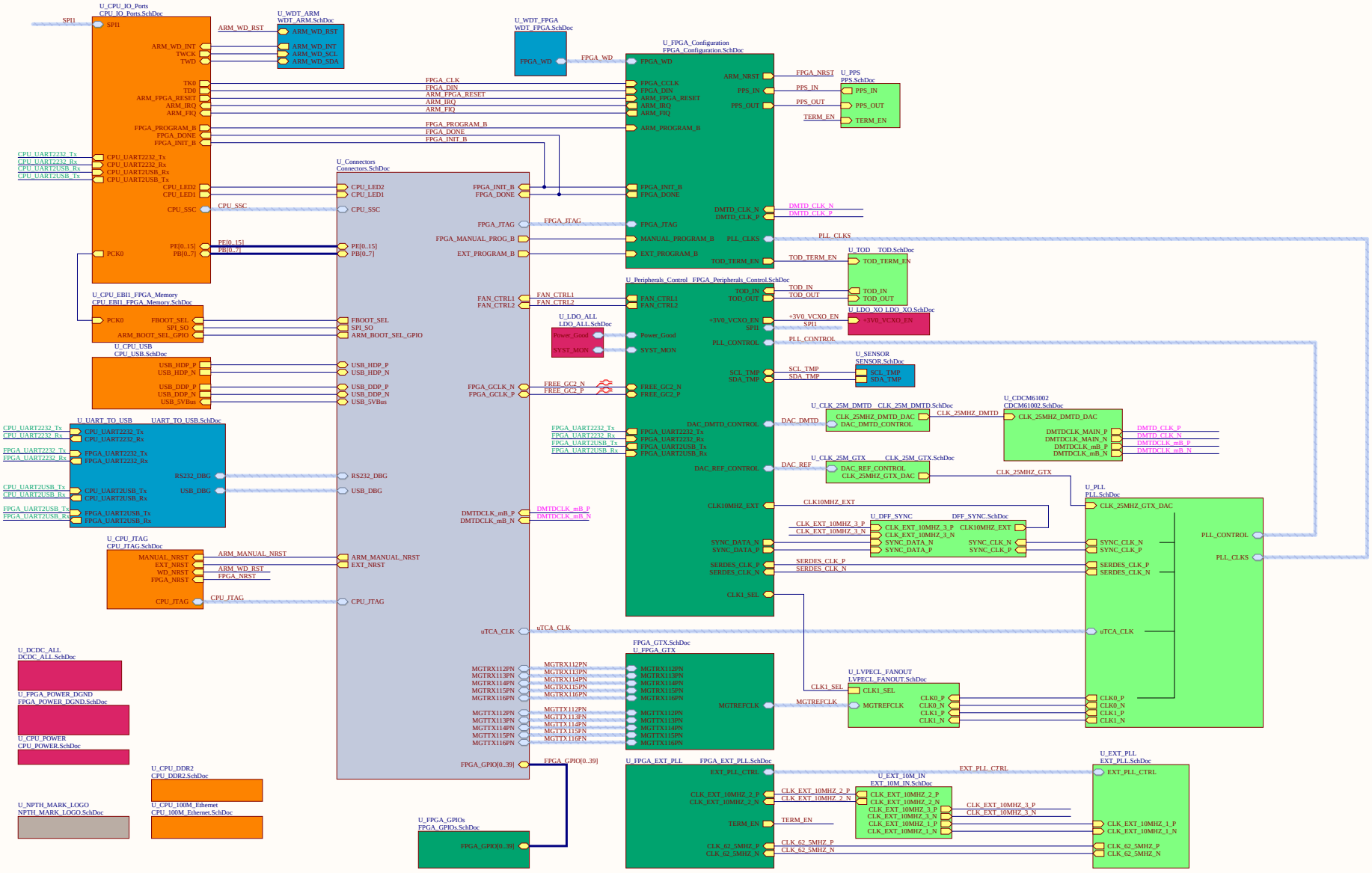
U_CPU_IO_Ports
CPU_IO_Ports.SchDoc
U_WDT_ARM
WDT_ARM.SchDoc
U_WDT_FPGA
WDT_FPGA.SchDoc
U_FPGA_Configuration
FPGA_Configuration.SchDoc
U_PPS
PPS.SchDoc
U_Connectors
Connectors.SchDoc
U_CPU_EBI1_FPGA_Memory
CPU_EBI1_FPGA_Memory.SchDoc
U_CPU_USB
CPU_USB.SchDoc
U_LDO_ALL
LDO_ALL.SchDoc
U_Peripherals_Control
FPGA_Peripherals_Control.SchDoc
U_TOD
TOD.SchDoc
U_LDO_XO
LDO_XO.SchDoc
U_SENSOR
SENSOR.SchDoc
U_CDCM61002
CDCM61002.SchDoc
U_CLK_25M_DMTD
CLK_25MHZ_DMTD.SchDoc
U_UART_TO_USB
UART_TO_USB.SchDoc
U_CLK_25M_GTX
CLK_25M_GTX.SchDoc
U_DFF_SYNC
DFF_SYNC.SchDoc
U_PLL
PLL.SchDoc
U_CPU_JTAG
CPU_JTAG.SchDoc
U_LVPECL_FANOUT
LVPECL_FANOUT.SchDoc
U_FPGA_GTX
FPGA_GTX.SchDoc
U_DCDC_ALL
DCDC_ALL.SchDoc
U_FPGA_POWER_DGND
FPGA_POWER_DGND.SchDoc
U_CPU_POWER
CPU_POWER.SchDoc
U_CPU_DDR2
CPU_DDR2.SchDoc
U_NPTH_MARK_LOGO
NPTH_MARK_LOGO.SchDoc
U_CPU_100M_Ethernet
CPU_100M_Ethernet.SchDoc
U_FPGA_GPIOs
FPGA_GPIOs.SchDoc
U_FPGA_EXT_PLL
FPGA_EXT_PLL.SchDoc
U_EXT_10M_IN
EXT_10M_IN.SchDoc
U_EXT_PLL
EXT_PLL.SchDoc
SPI1
ARM_WD_RST
ARM_WD_INT
TWCK
TWD
TK0
TD0
ARM_FPGA_RESET
ARM_IRQ
ARM_FIQ
FPGA_PROGRAM_B
FPGA_DONE
FPGA_INIT_B
CPU_UART2232_Tx
CPU_UART2232_Rx
CPU_UART2USB_Rx
CPU_UART2USB_Tx
CPU_LED2
CPU_LED1
CPU_SSC
PE[0..15]
PB[0..7]
PCK0
FBOOT_SEL
SPI_SO
ARM_BOOT_SEL_GPIO
USB_HDP_P
USB_HDP_N
USB_DDP_P
USB_DDP_N
USB_5VBus
FPGA_GCLK_N
FPGA_GCLK_P
FREE_GC2_N
FREE_GC2_P
FPGA_JTAG
FPGA_MANUAL_PROG_B
EXT_PROGRAM_B
FAN_CTRL1
FAN_CTRL2
Power_Good
SYST_MON
FPGA_UART2232_Tx
FPGA_UART2232_Rx
FPGA_UART2USB_Tx
FPGA_UART2USB_Rx
RS232_DBG
USB_DBG
DMTDCLK_mB_P
DMTDCLK_mB_N
MANUAL_NRST
EXT_NRST
WD_NRST
FPGA_NRST
ARM_MANUAL_NRST
ARM_WD_RST
CPU_JTAG
uTCA_CLK
FPGA_GPIO[0..39]
MGTRX112PN
MGTRX113PN
MGTRX114PN
MGTRX115PN
MGTRX116PN
MGTTX112PN
MGTTX113PN
MGTTX114PN
MGTTX115PN
MGTTX116PN
MGTREFCLK
ARM_NRST
PPS_IN
PPS_OUT
TERM_EN
DMTD_CLK_N
DMTD_CLK_P
PLL_CLKS
TOD_TERM_EN
TOD_IN
TOD_OUT
+3V0_VCXO_EN
SPI1
PLL_CONTROL
SCL_TMP
SDA_TMP
CLK_25MHZ_DMTD
DAC_DMTD
DAC_DMTD_CONTROL
DAC_REF
DAC_REF_CONTROL
CLK_25MHZ_GTX
CLK10MHZ_EXT
CLK_EXT_10MHZ_3_P
CLK_EXT_10MHZ_3_N
SYNC_DATA_N
SYNC_DATA_P
SERDES_CLK_P
SERDES_CLK_N
CLK1_SEL
CLK0_P
CLK0_N
CLK1_P
CLK1_N
EXT_PLL_CTRL
CLK_EXT_10MHZ_2_P
CLK_EXT_10MHZ_2_N
CLK_EXT_10MHZ_1_P
CLK_EXT_10MHZ_1_N
CLK_62_5MHZ_P
CLK_62_5MHZ_N
TERM_EN
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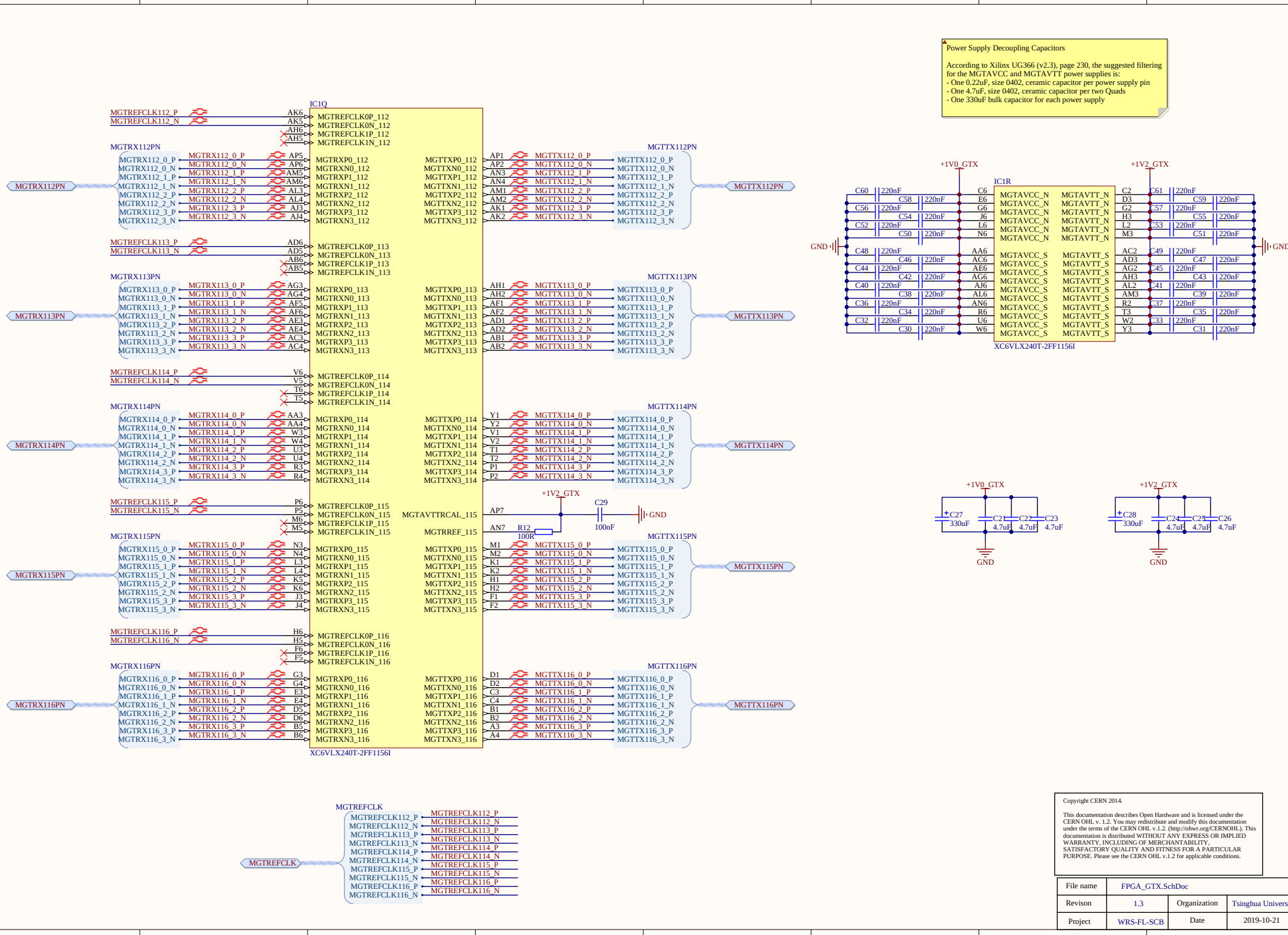
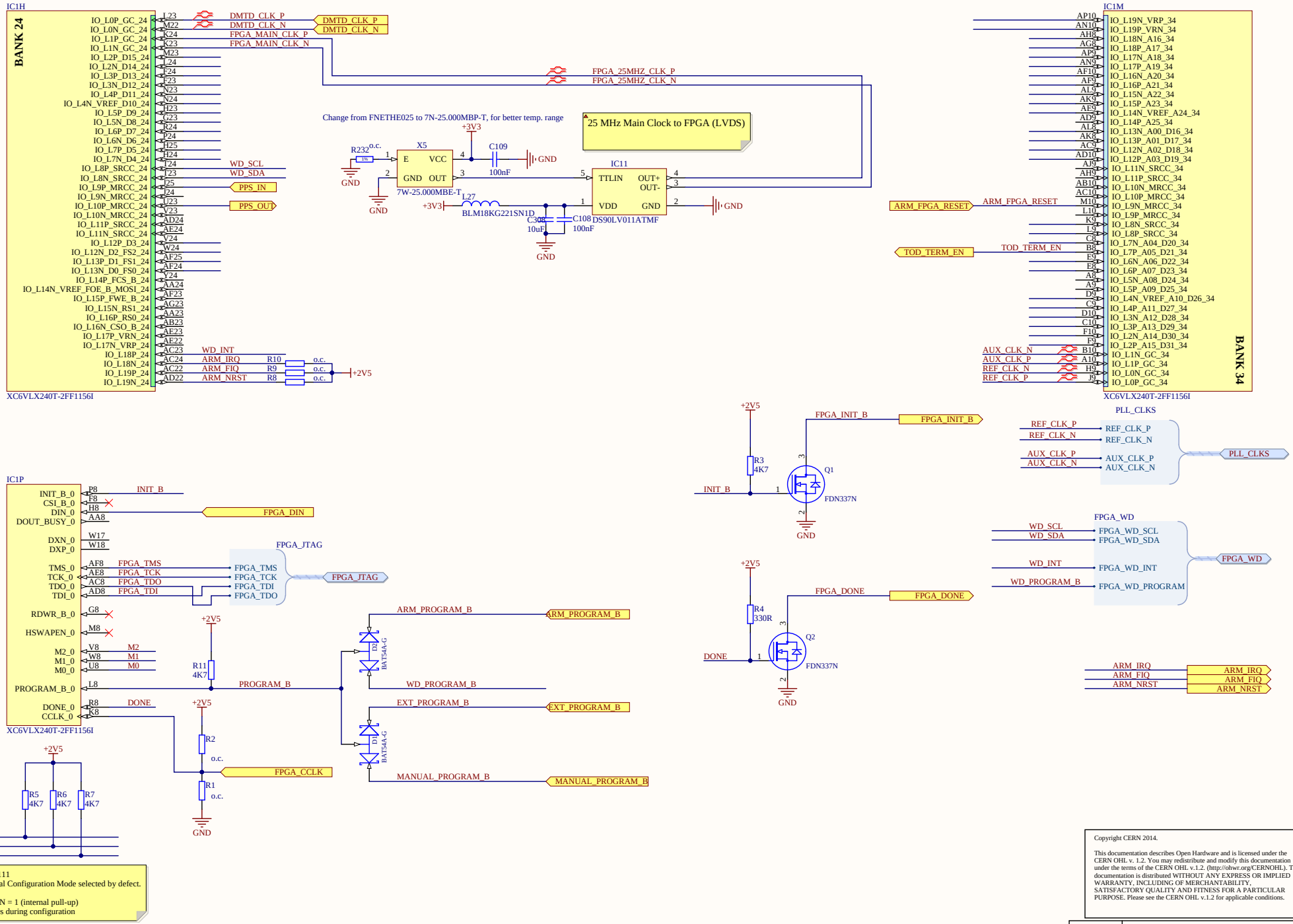
File name
SCB_MAIN.SchDoc
Revison
1.3
Organization
Tsinghua University
Project
WRS-FL-SCB
Date
2019-10-21



File name	FPGA_GTX.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21


IC1H
BANK 24
IO_L0P_GC_24
IO_L0N_GC_24
IO_L1P_GC_24
IO_L1N_GC_24
IO_L2P_D15_24
IO_L2N_D14_24
IO_L3P_D13_24
IO_L3N_D12_24
IO_L4P_D11_24
IO_L4N_VREF_D10_24
IO_L5P_D9_24
IO_L5N_D8_24
IO_L6P_D7_24
IO_L6N_D6_24
IO_L7P_D5_24
IO_L7N_D4_24
IO_L8P_SRCC_24
IO_L8N_SRCC_24
IO_L9P_MRCC_24
IO_L9N_MRCC_24
IO_L10P_MRCC_24
IO_L10N_MRCC_24
IO_L11P_SRCC_24
IO_L11N_SRCC_24
IO_L12P_D3_24
IO_L12N_D2_FS2_24
IO_L13P_D1_FS1_24
IO_L13N_D0_FS0_24
IO_L14P_FCS_B_24
IO_L14N_VREF_FOE_B_MOSI_24
IO_L15P_FWE_B_24
IO_L15N_RS1_24
IO_L16P_RS0_24
IO_L16N_CSO_B_24
IO_L17P_VRN_24
IO_L17N_VRP_24
IO_L18P_24
IO_L18N_24
IO_L19P_24
IO_L19N_24
DMTD_CLK_P
DMTD_CLK_N
FPGA_MAIN_CLK_P
FPGA_MAIN_CLK_N
WD_SCL
WD_SDA
PPS_IN
PPS_OUT
WD_INT
ARM_IRQ
ARM_FIQ
ARM_NRST
R10
R9
R8
o.c.
+2V5
XC6VLX240T-2FF1156I
FPGA_25MHZ_CLK_P
FPGA_25MHZ_CLK_N
Change from FNETHE025 to 7N-25.000MBP-T, for better temp. range
25 MHz Main Clock to FPGA (LVDS)
+3V3
R232
X5
E
VCC
GND
OUT
7W-25.000MBE-T
C109
100nF
IC11
TTLIN
OUT+
OUT-
VDD
GND
DS90LV011ATMF
L27
BLM18KG221SN1D
C30
10uF
C108
100nF
IC1M
BANK 34
IO_L19N_VRP_34
IO_L19P_VRN_34
IO_L18N_A16_34
IO_L18P_A17_34
IO_L17N_A18_34
IO_L17P_A19_34
IO_L16N_A20_34
IO_L16P_A21_34
IO_L15N_A22_34
IO_L15P_A23_34
IO_L14N_VREF_A24_34
IO_L14P_A25_34
IO_L13N_A00_D16_34
IO_L13P_A01_D17_34
IO_L12N_A02_D18_34
IO_L12P_A03_D19_34
IO_L11N_SRCC_34
IO_L11P_SRCC_34
IO_L10N_MRCC_34
IO_L10P_MRCC_34
IO_L9N_MRCC_34
IO_L9P_MRCC_34
IO_L8N_SRCC_34
IO_L8P_SRCC_34
IO_L7N_A04_D20_34
IO_L7P_A05_D21_34
IO_L6N_A06_D22_34
IO_L6P_A07_D23_34
IO_L5N_A08_D24_34
IO_L5P_A09_D25_34
IO_L4N_VREF_A10_D26_34
IO_L4P_A11_D27_34
IO_L3N_A12_D28_34
IO_L3P_A13_D29_34
IO_L2N_A14_D30_34
IO_L2P_A15_D31_34
IO_L1N_GC_34
IO_L1P_GC_34
IO_L0N_GC_34
IO_L0P_GC_34
ARM_FPGA_RESET
TOD_TERM_EN
AUX_CLK_N
AUX_CLK_P
REF_CLK_N
REF_CLK_P
XC6VLX240T-2FF1156I
IC1P
INIT_B_0
CSI_B_0
DIN_0
DOUT_BUSY_0
DXN_0
DXP_0
TMS_0
TCK_0
TDO_0
TDI_0
RDWR_B_0
HSWAPEN_0
M2_0
M1_0
M0_0
PROGRAM_B_0
DONE_0
CCLK_0
INIT_B
FPGA_DIN
FPGA_JTAG
FPGA_TMS
FPGA_TCK
FPGA_TDO
FPGA_TDI
R11
4K7
PROGRAM_B
DONE
R2
o.c.
R1
o.c.
FPGA_CCLK
R5
4K7
R6
4K7
R7
4K7
M2
M1
M0
D2
BAT54A-G
D1
BAT54A-G
ARM_PROGRAM_B
WD_PROGRAM_B
EXT_PROGRAM_B
MANUAL_PROGRAM_B
M[2:0] = 111
Slave Serial Configuration Mode selected by defect.
HSWAPEN = 1 (internal pull-up)
3-state I/Os during configuration
R3
4K7
Q1
FDN337N
FPGA_INIT_B
R4
330R
Q2
FPGA_DONE
PLL_CLKS
FPGA_WD
FPGA_WD_SCL
FPGA_WD_INT
FPGA_WD_PROGRAM
WD_PROGRAM_B
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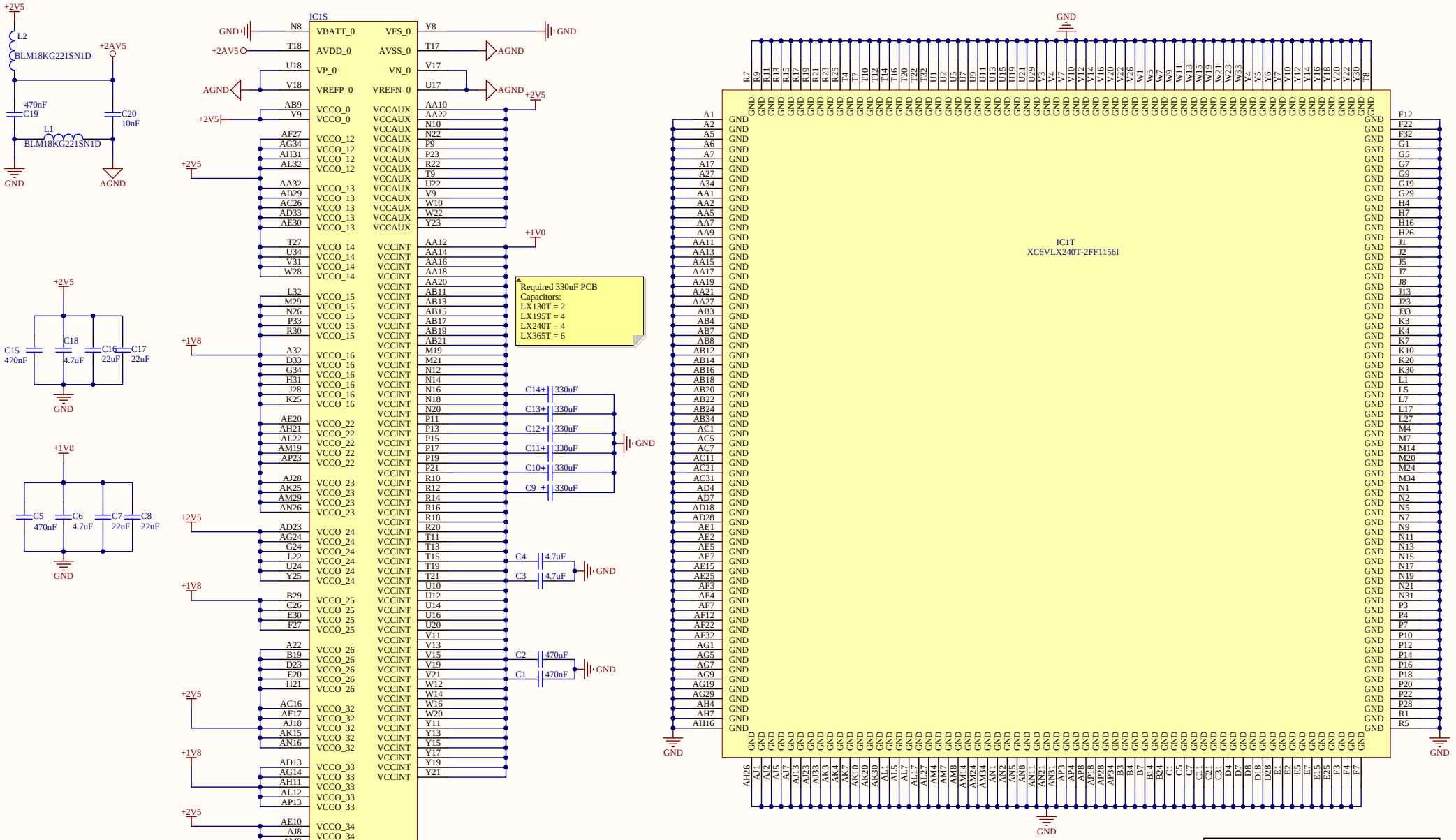
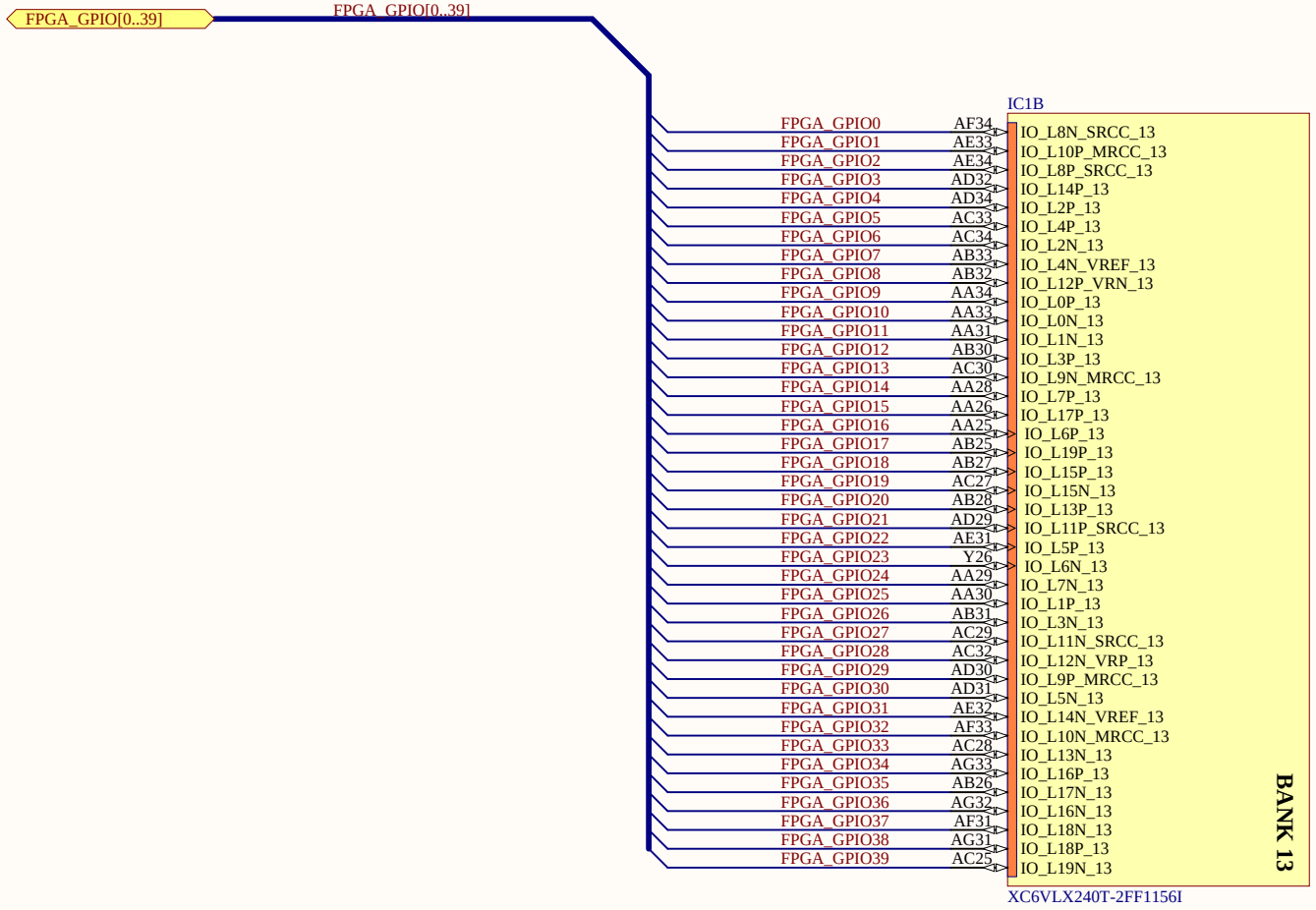
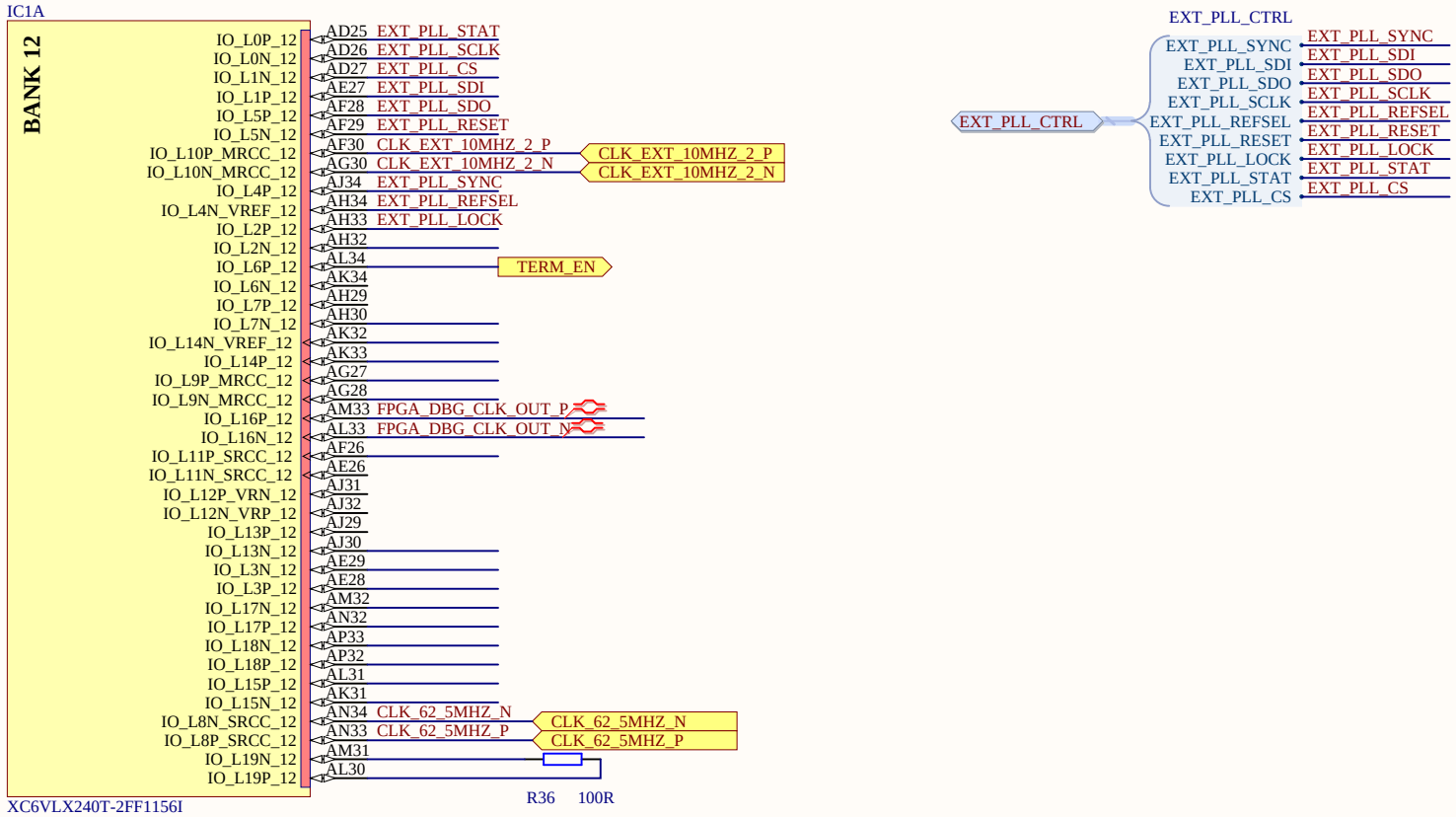
File name
FPGA_Configuration.SchDoc
Revison
1.3
Organization
Tsinghua University
Project
WRS-FL-SCB
Date
2019-10-21



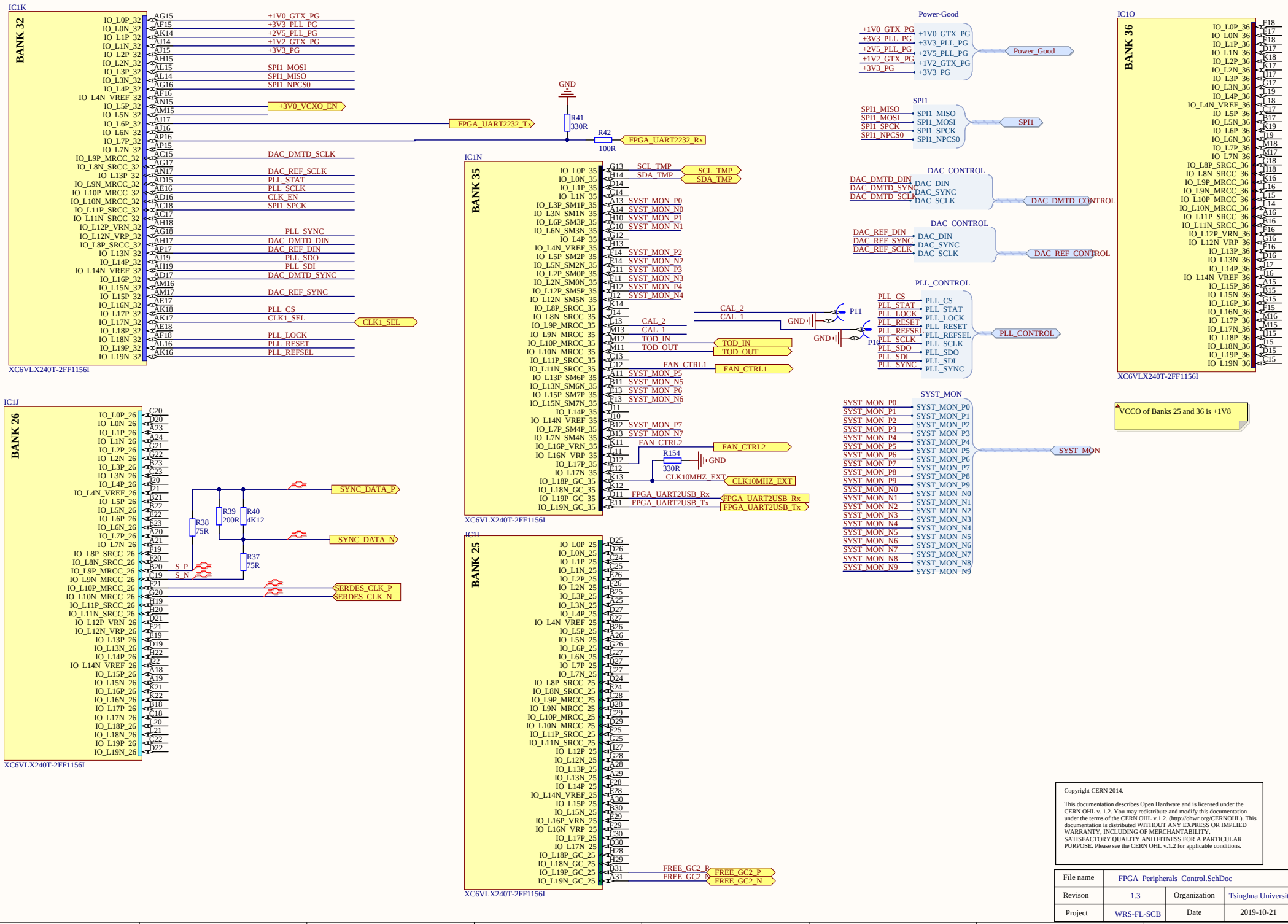
File name	FPGA_POWER_DGND.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



File name	FPGA_GPIOs.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



File name	FPGA_EXT_PLL.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21


IC1K
BANK 32
IO_L0P_32 AG15 +1V0_GTX_PG
IO_L0N_32 AF15 +3V3_PLL_PG
IO_L1P_32 AK14 +2V5_PLL_PG
IO_L1N_32 AJ14 +1V2_GTX_PG
IO_L2P_32 AJ15 +3V3_PG
IO_L2N_32 AH15
IO_L3P_32 AL15 SPI1_MOSI
IO_L3N_32 AL14 SPI1_MISO
IO_L4P_32 AG16 SPI1_NPCS0
IO_L4N_VREF_32 AF16
IO_L5P_32 AN15
IO_L5N_32 AM15 +3V0_VCXO_EN
IO_L6P_32 AJ17 FPGA_UART2232_Tx
IO_L6N_32 AJ16
IO_L7P_32 AP16 FPGA_UART2232_Rx
IO_L7N_32 AP15
IO_L9P_MRCC_32 AC15 DAC_DMTD_SCLK
IO_L8N_SRCC_32 AG17
IO_L13P_32 AN17 DAC_REF_SCLK
IO_L9N_MRCC_32 AD15 PLL_STAT
IO_L10P_MRCC_32 AE16 PLL_SCLK
IO_L10N_MRCC_32 AD16 CLK_EN
IO_L11P_SRCC_32 AC18 SPI1_SPCK
IO_L11N_SRCC_32 AC17
IO_L12P_VRN_32 AH18
IO_L12N_VRP_32 AG18 PLL_SYNC
IO_L8P_SRCC_32 AH17 DAC_DMTD_DIN
IO_L13N_32 AP17 DAC_REF_DIN
IO_L14P_32 AJ19 PLL_SDO
IO_L14N_VREF_32 AH19 PLL_SDI
IO_L16P_32 AD17 DAC_DMTD_SYNC
IO_L15N_32 AM16
IO_L15P_32 AM17 DAC_REF_SYNC
IO_L16N_32 AE17
IO_L17P_32 AK18 PLL_CS
IO_L17N_32 AK17 CLK1_SEL
IO_L18P_32 AE18
IO_L18N_32 AF18 PLL_LOCK
IO_L19P_32 AL16 PLL_RESET
IO_L19N_32 AK16 PLL_REFSEL
XC6VLX240T-2FF1156I
GND
R41 330R
R42 100R
IC1N
BANK 35
IO_L0P_35 G13 SCL_TMP SCL_TMP
IO_L0N_35 H14 SDA_TMP SDA_TMP
IO_L1P_35 D14
IO_L1N_35 C14
IO_L3P_SM1P_35 A13 SYST_MON_P0
IO_L3N_SM1N_35 A14 SYST_MON_N0
IO_L6P_SM3P_35 H10 SYST_MON_P1
IO_L6N_SM3N_35 G10 SYST_MON_N1
IO_L4P_35 G12
IO_L4N_VREF_35 H13
IO_L5P_SM2P_35 F14 SYST_MON_P2
IO_L5N_SM2N_35 E14 SYST_MON_N2
IO_L2P_SM0P_35 G11 SYST_MON_P3
IO_L2N_SM0N_35 F11 SYST_MON_N3
IO_L12P_SM5P_35 H12 SYST_MON_P4
IO_L12N_SM5N_35 J12 SYST_MON_N4
IO_L8P_SRCC_35 K14
IO_L8N_SRCC_35 J14 CAL_2
IO_L9P_MRCC_35 L13 CAL_2
IO_L9N_MRCC_35 M13 CAL_1
IO_L10P_MRCC_35 M12 TOD_IN TOD_IN
IO_L10N_MRCC_35 M11 TOD_OUT TOD_OUT
IO_L11P_SRCC_35 C13
IO_L11N_SRCC_35 C12 FAN_CTRL1 FAN_CTRL1
IO_L13P_SM6P_35 A11 SYST_MON_P5
IO_L13N_SM6N_35 B11 SYST_MON_N5
IO_L15P_SM7P_35 F13 SYST_MON_P6
IO_L15N_SM7N_35 F13 SYST_MON_N6
IO_L14P_35 J11
IO_L14N_VREF_35 J10
IO_L7P_SM4P_35 B12 SYST_MON_P7
IO_L7N_SM4N_35 B13 SYST_MON_N7
IO_L16P_VRN_35 K11 FAN_CTRL2 FAN_CTRL2
IO_L16N_VRP_35 L11
IO_L17P_35 D12 R154 330R GND
IO_L17N_35 E12
IO_L18P_GC_35 K13 CLK10MHZ_EXT CLK10MHZ_EXT
IO_L18N_GC_35 K12
IO_L19P_GC_35 D11 FPGA_UART2USB_Rx FPGA_UART2USB_Rx
IO_L19N_GC_35 E11 FPGA_UART2USB_Tx FPGA_UART2USB_Tx
XC6VLX240T-2FF1156I
P11
P10
GND
GND
IC1J
BANK 26
IO_L0P_26 C20
IO_L0N_26 D20
IO_L1P_26 A23
IO_L1N_26 A24
IO_L2P_26 G21
IO_L2N_26 G22
IO_L3P_26 B23
IO_L3N_26 C23
IO_L4P_26 J20
IO_L4N_VREF_26 J21
IO_L5P_26 B21
IO_L5N_26 B22
IO_L6P_26 E22
IO_L6N_26 E23
IO_L7P_26 A20
IO_L7N_26 A21
IO_L8P_SRCC_26 F19
IO_L8N_SRCC_26 F20
IO_L9P_MRCC_26 B20 S_P
IO_L9N_MRCC_26 C19 S_N
IO_L10P_MRCC_26 G21
IO_L10N_MRCC_26 G20
IO_L11P_SRCC_26 H19
IO_L11N_SRCC_26 H20
IO_L12P_VRN_26 D21
IO_L12N_VRP_26 E21
IO_L13P_26 E19
IO_L13N_26 D19
IO_L14P_26 H22
IO_L14N_VREF_26 J22
IO_L15P_26 A18
IO_L15N_26 A19
IO_L16P_26 K21
IO_L16N_26 K22
IO_L17P_26 B18
IO_L17N_26 C18
IO_L18P_26 L20
IO_L18N_26 L21
IO_L19P_26 C22
IO_L19N_26 D22
XC6VLX240T-2FF1156I
R38 75R
R39 200R
R40 4K12
R37 75R
SYNC_DATA_P
SYNC_DATA_N
SERDES_CLK_P
SERDES_CLK_N
IC1H
BANK 25
IO_L0P_25 D25
IO_L0N_25 D26
IO_L1P_25 C24
IO_L1N_25 C25
IO_L2P_25 E26
IO_L2N_25 F26
IO_L3P_25 B25
IO_L3N_25 A25
IO_L4P_25 D27
IO_L4N_VREF_25 E27
IO_L5P_25 B26
IO_L5N_25 A26
IO_L6P_25 G26
IO_L6N_25 G27
IO_L7P_25 B27
IO_L7N_25 C27
IO_L8P_SRCC_25 D24
IO_L8N_SRCC_25 F24
IO_L9P_MRCC_25 C28
IO_L9N_MRCC_25 B28
IO_L10P_MRCC_25 C29
IO_L10N_MRCC_25 D29
IO_L11P_SRCC_25 E25
IO_L11N_SRCC_25 G25
IO_L12P_25 H27
IO_L12N_25 G28
IO_L13P_25 A28
IO_L13N_25 A29
IO_L14P_25 F28
IO_L14N_VREF_25 E28
IO_L15P_25 A30
IO_L15N_25 B30
IO_L16P_VRN_25 F29
IO_L16N_VRP_25 E29
IO_L17P_25 C30
IO_L17N_25 D30
IO_L18P_GC_25 H28
IO_L18N_GC_25 H29
IO_L19P_GC_25 B31 FREE_GC2_P FREE_GC2_P
IO_L19N_GC_25 A31 FREE_GC2 FREE_GC2_N
XC6VLX240T-2FF1156I
Power-Good
+1V0_GTX_PG +1V0_GTX_PG
+3V3_PLL_PG +3V3_PLL_PG
+2V5_PLL_PG +2V5_PLL_PG
+1V2_GTX_PG +1V2_GTX_PG
+3V3_PG +3V3_PG
Power_Good
SPI1
SPI1_MISO SPI1_MISO
SPI1_MOSI SPI1_MOSI
SPI1_SPCK SPI1_SPCK
SPI1_NPCS0 SPI1_NPCS0
SPI1
DAC_CONTROL
DAC_DMTD_DIN DAC_DIN
DAC_DMTD_SYNC DAC_SYNC
DAC_DMTD_SCLK DAC_SCLK
DAC_DMTD_CONTROL
DAC_CONTROL
DAC_REF_DIN DAC_DIN
DAC_REF_SYNC DAC_SYNC
DAC_REF_SCLK DAC_SCLK
DAC_REF_CONTROL
PLL_CONTROL
PLL_CS PLL_CS
PLL_STAT PLL_STAT
PLL_LOCK PLL_LOCK
PLL_RESET PLL_RESET
PLL_REFSEL PLL_REFSEL
PLL_SCLK PLL_SCLK
PLL_SDO PLL_SDO
PLL_SDI PLL_SDI
PLL_SYNC PLL_SYNC
PLL_CONTROL
SYST_MON
SYST_MON_P0 SYST_MON_P0
SYST_MON_P1 SYST_MON_P1
SYST_MON_P2 SYST_MON_P2
SYST_MON_P3 SYST_MON_P3
SYST_MON_P4 SYST_MON_P4
SYST_MON_P5 SYST_MON_P5
SYST_MON_P6 SYST_MON_P6
SYST_MON_P7 SYST_MON_P7
SYST_MON_P8 SYST_MON_P8
SYST_MON_P9 SYST_MON_P9
SYST_MON_N0 SYST_MON_N0
SYST_MON_N1 SYST_MON_N1
SYST_MON_N2 SYST_MON_N2
SYST_MON_N3 SYST_MON_N3
SYST_MON_N4 SYST_MON_N4
SYST_MON_N5 SYST_MON_N5
SYST_MON_N6 SYST_MON_N6
SYST_MON_N7 SYST_MON_N7
SYST_MON_N8 SYST_MON_N8
SYST_MON_N9 SYST_MON_N9
SYST_MON
IC1O
BANK 36
IO_L0P_36 F18
IO_L0N_36 E17
IO_L1P_36 E18
IO_L1N_36 D17
IO_L2P_36 K18
IO_L2N_36 K17
IO_L3P_36 H17
IO_L3N_36 G17
IO_L4P_36 L19
IO_L4N_VREF_36 L18
IO_L5P_36 C17
IO_L5N_36 B17
IO_L6P_36 K19
IO_L6N_36 J19
IO_L7P_36 M18
IO_L7N_36 M17
IO_L8P_SRCC_36 G18
IO_L8N_SRCC_36 H18
IO_L9P_MRCC_36 K16
IO_L9N_MRCC_36 L16
IO_L10P_MRCC_36 L15
IO_L10N_MRCC_36 L14
IO_L11P_SRCC_36 A16
IO_L11N_SRCC_36 B16
IO_L12P_VRN_36 F16
IO_L12N_VRP_36 G16
IO_L13P_36 E16
IO_L13N_36 D16
IO_L14P_36 J17
IO_L14N_VREF_36 J16
IO_L15P_36 A15
IO_L15N_36 B15
IO_L16P_36 E15
IO_L16N_36 F15
IO_L17P_36 M16
IO_L17N_36 M15
IO_L18P_36 A15
IO_L18N_36 B15
IO_L19P_36 E15
IO_L19N_36 F15
XC6VLX240T-2FF1156I
VCCO of Banks 25 and 36 is +1V8
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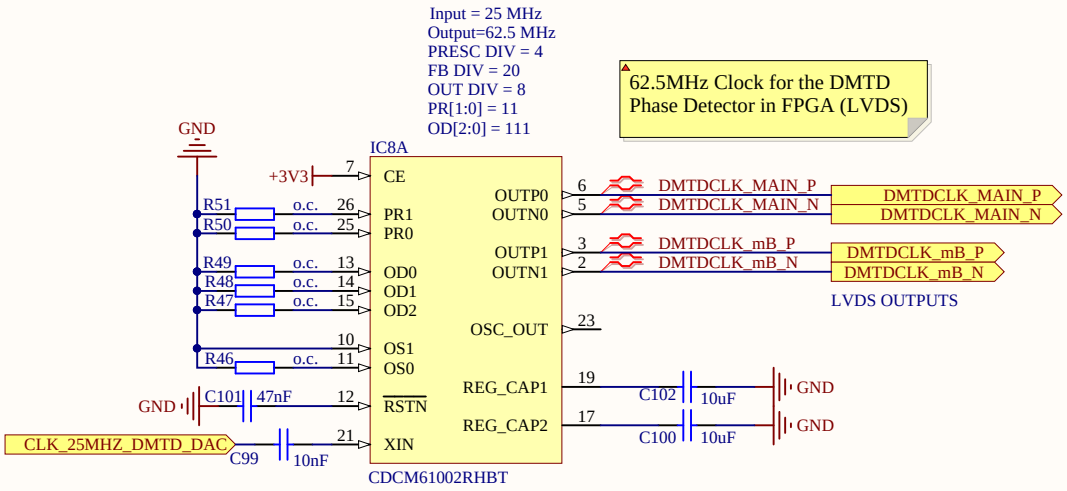
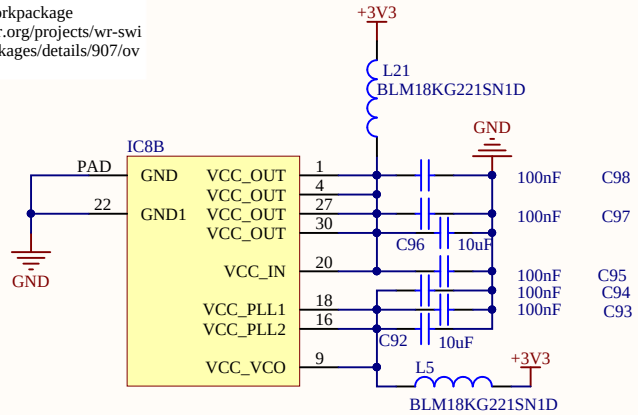
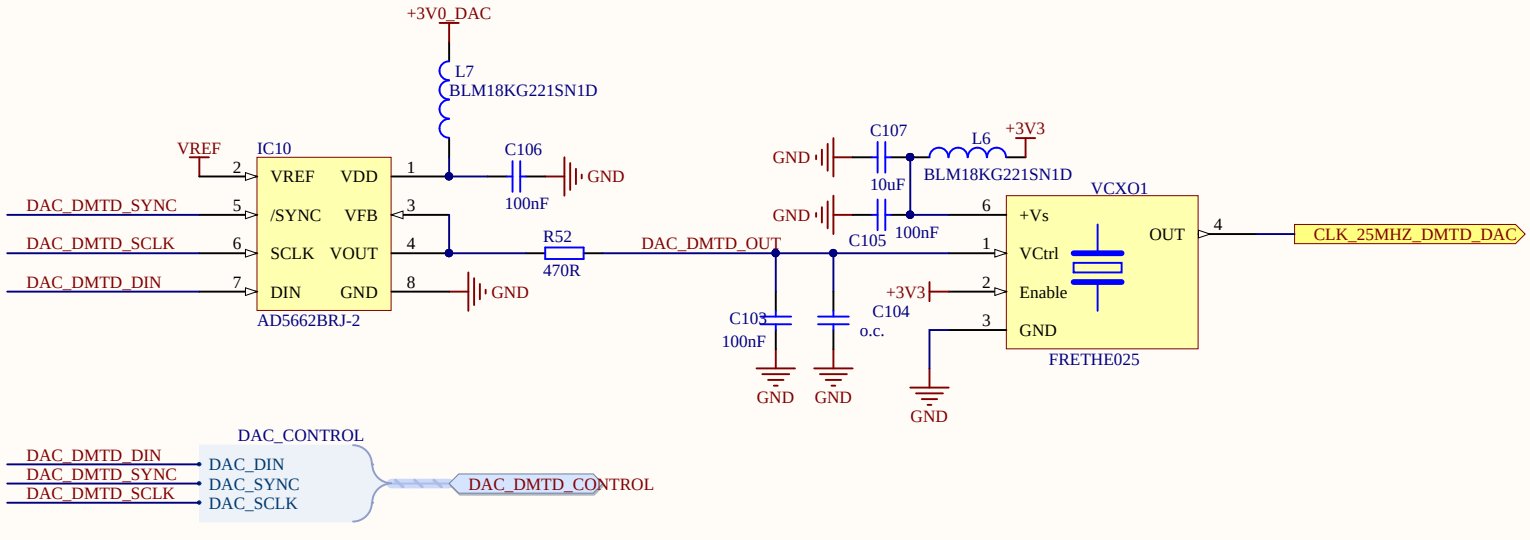
File name FPGA_Peripherals_Control.SchDoc
Revison 1.3
Organization Tsinghua University
Project WRS-FL-SCB
Date 2019-10-21



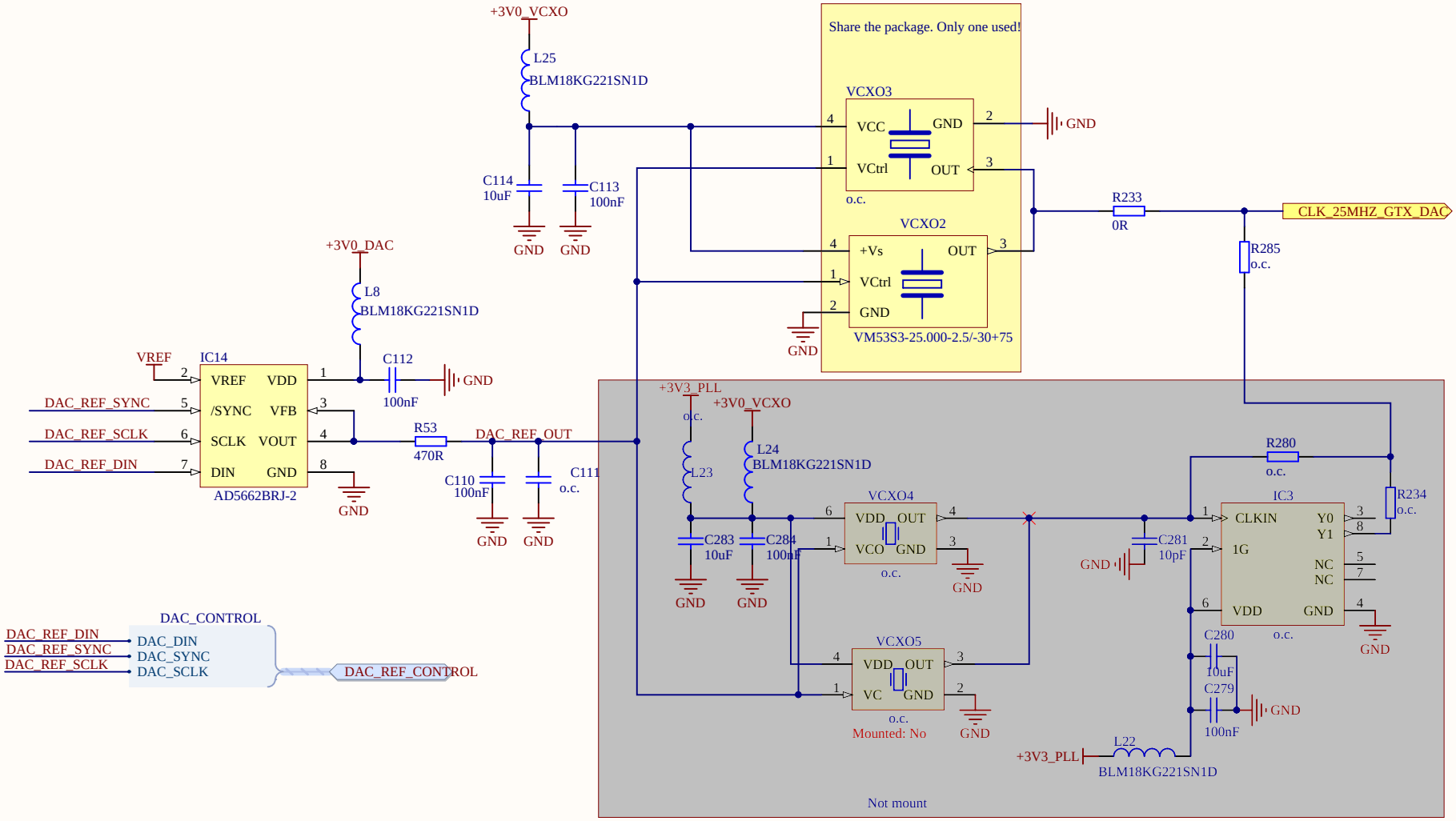
Change C101 to bigger value, to increase the reset time.
Refer to WRS-workpackage https://www.ohwr.org/projects/wr-switch-hw/work_packages/details/907/overview



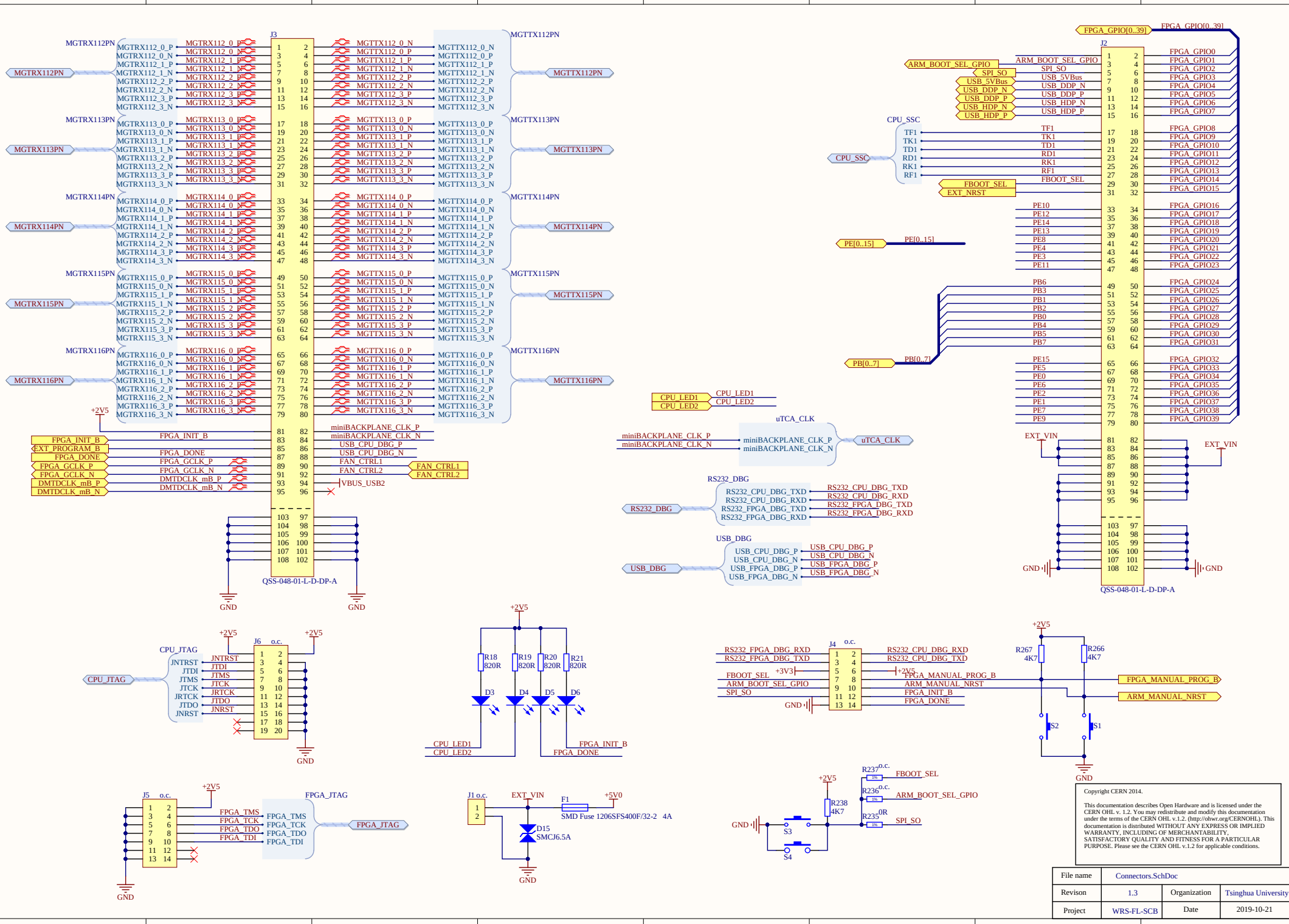
File name	CDCM61002.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



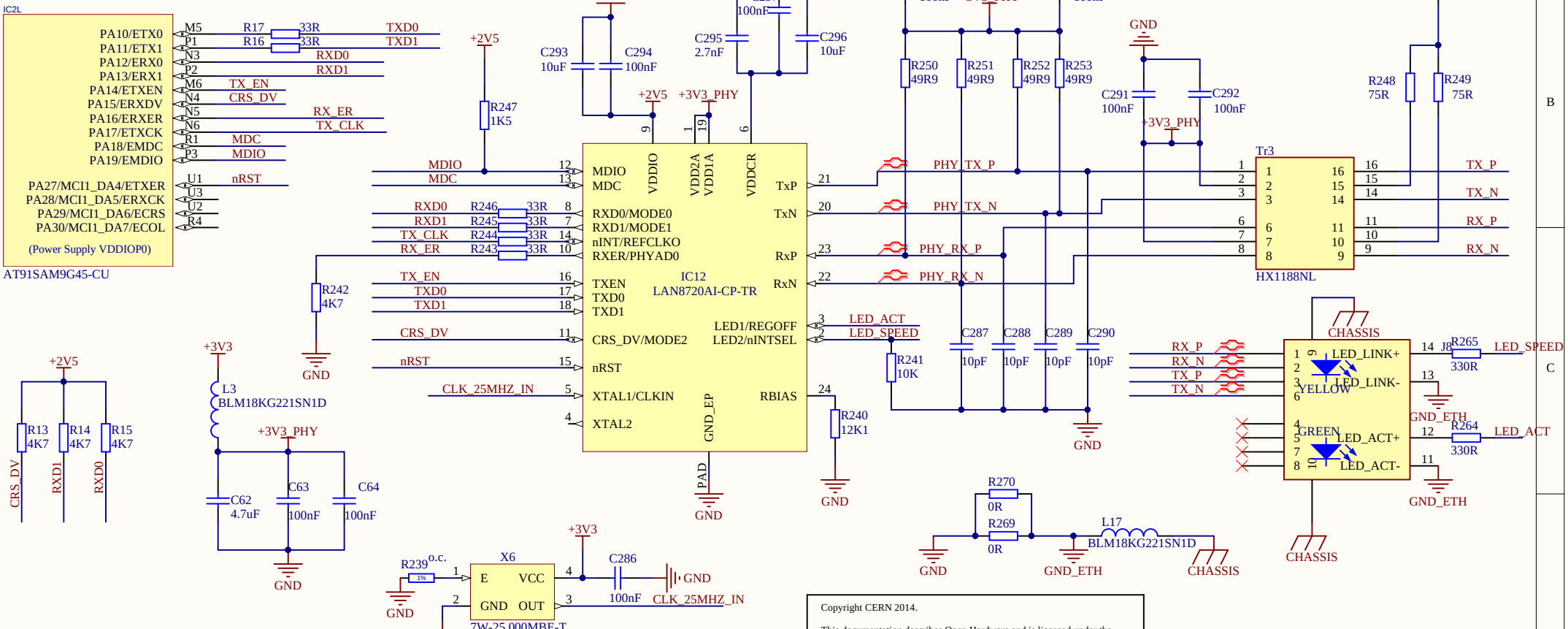
File name	CLK_25M_DMTD.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



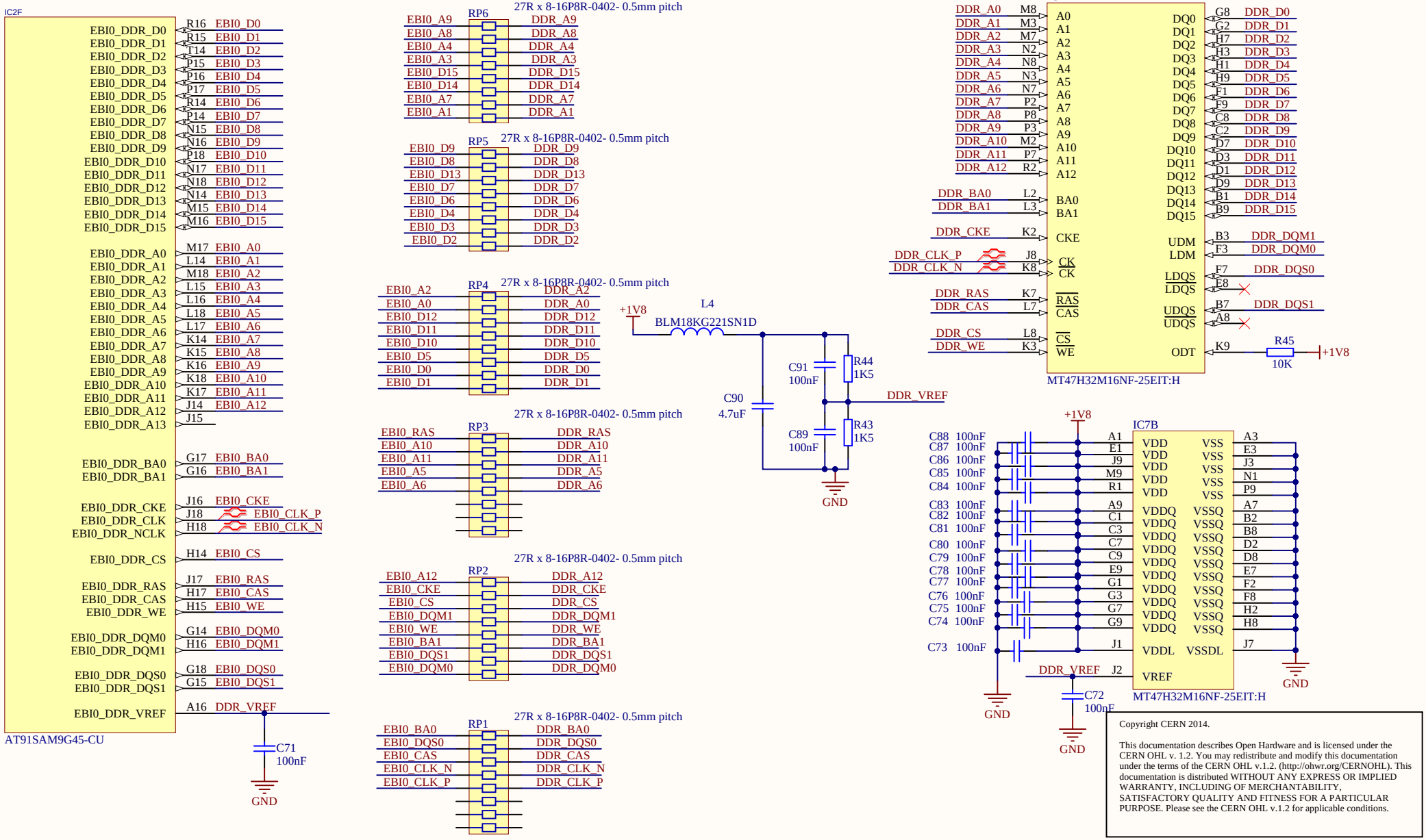
File name	CLK_25M_GTX.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



File name	Connectors.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



File name	CPU_100M_Ethernet.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21


IC2F
AT91SAM9G45-CU
EBI0_DDR_D0 R16 EBI0_D0
EBI0_DDR_D1 R15 EBI0_D1
EBI0_DDR_D2 T14 EBI0_D2
EBI0_DDR_D3 P15 EBI0_D3
EBI0_DDR_D4 P16 EBI0_D4
EBI0_DDR_D5 P17 EBI0_D5
EBI0_DDR_D6 R14 EBI0_D6
EBI0_DDR_D7 P14 EBI0_D7
EBI0_DDR_D8 N15 EBI0_D8
EBI0_DDR_D9 N16 EBI0_D9
EBI0_DDR_D10 P18 EBI0_D10
EBI0_DDR_D11 N17 EBI0_D11
EBI0_DDR_D12 N18 EBI0_D12
EBI0_DDR_D13 N14 EBI0_D13
EBI0_DDR_D14 M15 EBI0_D14
EBI0_DDR_D15 M16 EBI0_D15
EBI0_DDR_A0 M17 EBI0_A0
EBI0_DDR_A1 L14 EBI0_A1
EBI0_DDR_A2 M18 EBI0_A2
EBI0_DDR_A3 L15 EBI0_A3
EBI0_DDR_A4 L16 EBI0_A4
EBI0_DDR_A5 L18 EBI0_A5
EBI0_DDR_A6 L17 EBI0_A6
EBI0_DDR_A7 K14 EBI0_A7
EBI0_DDR_A8 K15 EBI0_A8
EBI0_DDR_A9 K16 EBI0_A9
EBI0_DDR_A10 K18 EBI0_A10
EBI0_DDR_A11 K17 EBI0_A11
EBI0_DDR_A12 J14 EBI0_A12
EBI0_DDR_A13 J15
EBI0_DDR_BA0 G17 EBI0_BA0
EBI0_DDR_BA1 G16 EBI0_BA1
EBI0_DDR_CKE J16 EBI0_CKE
EBI0_DDR_CLK J18 EBI0_CLK_P
EBI0_DDR_NCLK H18 EBI0_CLK_N
EBI0_DDR_CS H14 EBI0_CS
EBI0_DDR_RAS J17 EBI0_RAS
EBI0_DDR_CAS H17 EBI0_CAS
EBI0_DDR_WE H15 EBI0_WE
EBI0_DDR_DQM0 G14 EBI0_DQM0
EBI0_DDR_DQM1 H16 EBI0_DQM1
EBI0_DDR_DQS0 G18 EBI0_DQS0
EBI0_DDR_DQS1 G15 EBI0_DQS1
EBI0_DDR_VREF A16 DDR_VREF
C71
100nF
GND
RP6
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_A9 DDR_A9
EBI0_A8 DDR_A8
EBI0_A4 DDR_A4
EBI0_A3 DDR_A3
EBI0_D15 DDR_D15
EBI0_D14 DDR_D14
EBI0_A7 DDR_A7
EBI0_A1 DDR_A1
RP5
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_D9 DDR_D9
EBI0_D8 DDR_D8
EBI0_D13 DDR_D13
EBI0_D7 DDR_D7
EBI0_D6 DDR_D6
EBI0_D4 DDR_D4
EBI0_D3 DDR_D3
EBI0_D2 DDR_D2
RP4
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_A2 DDR_A2
EBI0_A0 DDR_A0
EBI0_D12 DDR_D12
EBI0_D11 DDR_D11
EBI0_D10 DDR_D10
EBI0_D5 DDR_D5
EBI0_D0 DDR_D0
EBI0_D1 DDR_D1
+1V8
L4
BLM18KG221SN1D
C91
100nF
C90
4.7uF
C89
100nF
R44
1K5
R43
1K5
DDR_VREF
GND
RP3
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_RAS DDR_RAS
EBI0_A10 DDR_A10
EBI0_A11 DDR_A11
EBI0_A5 DDR_A5
EBI0_A6 DDR_A6
RP2
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_A12 DDR_A12
EBI0_CKE DDR_CKE
EBI0_CS DDR_CS
EBI0_DQM1 DDR_DQM1
EBI0_WE DDR_WE
EBI0_BA1 DDR_BA1
EBI0_DQS1 DDR_DQS1
EBI0_DQM0 DDR_DQM0
RP1
27R x 8-16P8R-0402- 0.5mm pitch
EBI0_BA0 DDR_BA0
EBI0_DQS0 DDR_DQS0
EBI0_CAS DDR_CAS
EBI0_CLK_N DDR_CLK_N
EBI0_CLK_P DDR_CLK_P
IC7A
MT47H32M16NF-25EIT:H
DDR_A0 M8 A0
DDR_A1 M3 A1
DDR_A2 M7 A2
DDR_A3 N2 A3
DDR_A4 N8 A4
DDR_A5 N3 A5
DDR_A6 N7 A6
DDR_A7 P2 A7
DDR_A8 P8 A8
DDR_A9 P3 A9
DDR_A10 M2 A10
DDR_A11 P7 A11
DDR_A12 R2 A12
DDR_BA0 L2 BA0
DDR_BA1 L3 BA1
DDR_CKE K2 CKE
DDR_CLK_P J8 CK
DDR_CLK_N K8 CK
DDR_RAS K7 RAS
DDR_CAS L7 CAS
DDR_CS L8 CS
DDR_WE K3 WE
DQ0 G8 DDR_D0
DQ1 G2 DDR_D1
DQ2 H7 DDR_D2
DQ3 H3 DDR_D3
DQ4 H1 DDR_D4
DQ5 H9 DDR_D5
DQ6 F1 DDR_D6
DQ7 F9 DDR_D7
DQ8 C8 DDR_D8
DQ9 C2 DDR_D9
DQ10 D7 DDR_D10
DQ11 D3 DDR_D11
DQ12 D1 DDR_D12
DQ13 D9 DDR_D13
DQ14 B1 DDR_D14
DQ15 B9 DDR_D15
UDM B3 DDR_DQM1
LDM F3 DDR_DQM0
LDQS F7 DDR_DQS0
LDQS E8
UDQS B7 DDR_DQS1
UDQS A8
ODT K9
R45
10K
+1V8
IC7B
MT47H32M16NF-25EIT:H
C88 100nF
C87 100nF
C86 100nF
C85 100nF
C84 100nF
C83 100nF
C82 100nF
C81 100nF
C80 100nF
C79 100nF
C78 100nF
C77 100nF
C76 100nF
C75 100nF
C74 100nF
C73 100nF
VDD A1
VDD E1
VDD J9
VDD M9
VDD R1
VDDQ A9
VDDQ C1
VDDQ C3
VDDQ C7
VDDQ C9
VDDQ E9
VDDQ G1
VDDQ G3
VDDQ G7
VDDQ G9
VDDQ J1
VDDL
VREF J2
VSS A3
VSS E3
VSS J3
VSS N1
VSS P9
VSSQ A7
VSSQ B2
VSSQ B8
VSSQ D2
VSSQ D8
VSSQ E7
VSSQ F2
VSSQ F8
VSSQ H2
VSSQ H8
VSSDL J7
+1V8
DDR_VREF
C72
100nF
GND
GND
GND
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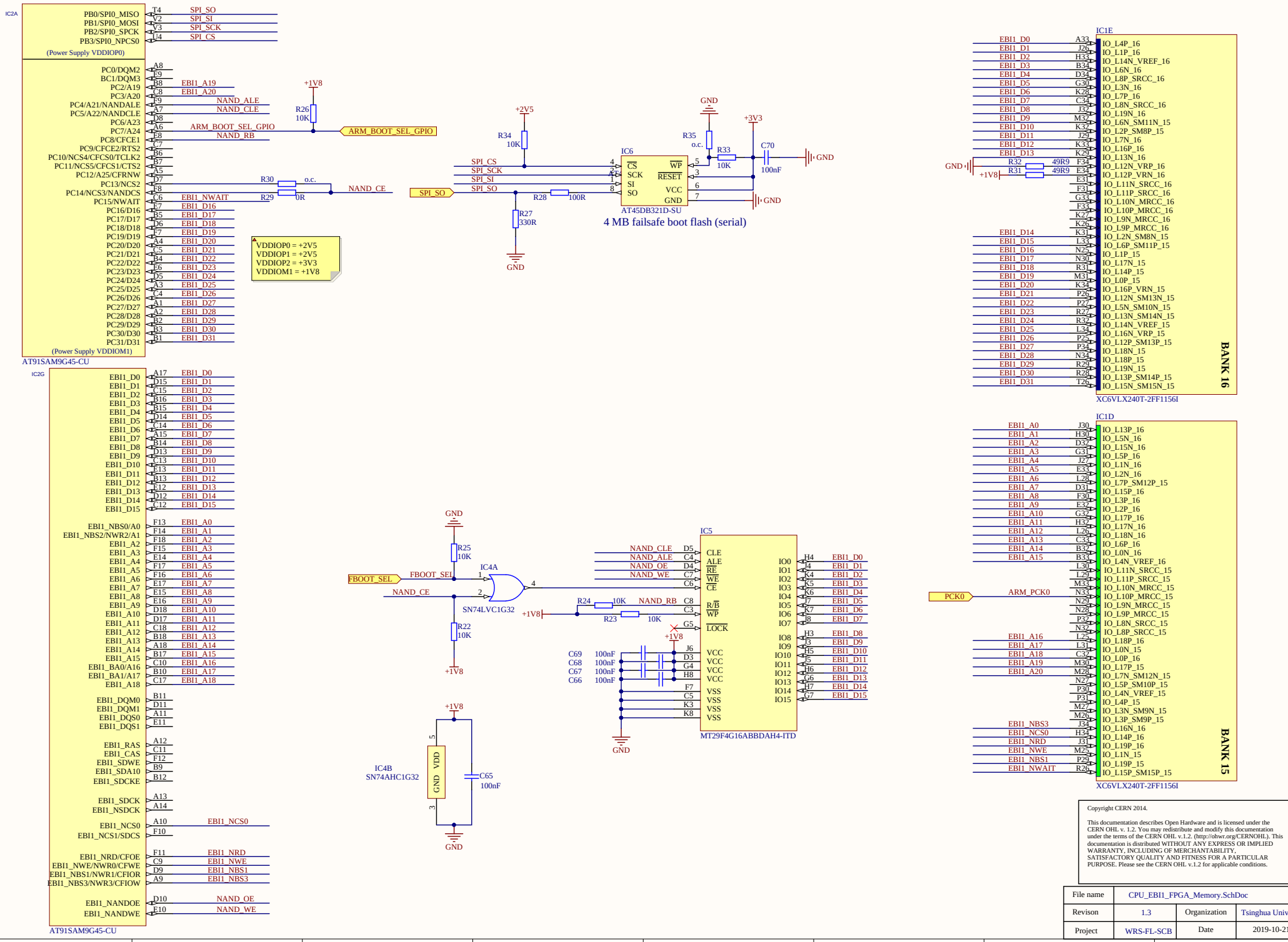
File name CPU_DDR2.SchDoc
Revison 1.3
Organization Tsinghua University
Project WRS-FL-SCB
Date 2019-10-21


IC2A
PB0/SPI0_MISO
PB1/SPI0_MOSI
PB2/SPI0_SPCK
PB3/SPI0_NPCS0
(Power Supply VDDIOP0)
PC0/DQM2
PC1/DQM3
PC2/A19
PC3/A20
PC4/A21/NANDALE
PC5/A22/NANDCLE
PC6/A23
PC7/A24
PC8/CFCE1
PC9/CFCE2/RTS2
PC10/NCS4/CFCS0/TCLK2
PC11/NCS5/CFCS1/CTS2
PC12/A25/CFRNW
PC13/NCS2
PC14/NCS3/NANDCS
PC15/NWAIT
PC16/D16
PC17/D17
PC18/D18
PC19/D19
PC20/D20
PC21/D21
PC22/D22
PC23/D23
PC24/D24
PC25/D25
PC26/D26
PC27/D27
PC28/D28
PC29/D29
PC30/D30
PC31/D31
(Power Supply VDDIOM1)
AT91SAM9G45-CU
SPI_SO
SPI_SI
SPI_SCK
SPI_CS
EBI1_A19
EBI1_A20
NAND_ALE
NAND_CLE
NAND_RB
ARM_BOOT_SEL_GPIO
R26 10K
+1V8
R30 o.c.
R29 0R
NAND_CE
EBI1_NWAIT
EBI1_D16
EBI1_D17
EBI1_D18
EBI1_D19
EBI1_D20
EBI1_D21
EBI1_D22
EBI1_D23
EBI1_D24
EBI1_D25
EBI1_D26
EBI1_D27
EBI1_D28
EBI1_D29
EBI1_D30
EBI1_D31
VDDIOP0 = +2V5
VDDIOP1 = +2V5
VDDIOP2 = +3V3
VDDIOM1 = +1V8
+2V5
R34 10K
SPI_CS
SPI_SCK
SPI_SI
SPI_SO
R28 100R
R27 330R
GND
IC6
CS
SCK
SI
SO
WP
RESET
VCC
GND
AT45DB321D-SU
4 MB failsafe boot flash (serial)
+3V3
R35 o.c.
R33 10K
C70 100nF
IC1E
EBI1_D0 A33
EBI1_D1 J26
EBI1_D2 H33
EBI1_D3 B34
EBI1_D4 D34
EBI1_D5 G30
EBI1_D6 K28
EBI1_D7 C34
EBI1_D8 J32
EBI1_D9 M32
EBI1_D10 K32
EBI1_D11 J29
EBI1_D12 K33
EBI1_D13 K29
R32 49R9 F34
R31 49R9 E34
E31
F31
G33
F33
K27
K26
EBI1_D14 K31
EBI1_D15 L33
EBI1_D16 N25
EBI1_D17 N30
EBI1_D18 R31
EBI1_D19 M31
EBI1_D20 K34
EBI1_D21 P26
EBI1_D22 P27
EBI1_D23 R27
EBI1_D24 R32
EBI1_D25 L34
EBI1_D26 P25
EBI1_D27 P34
EBI1_D28 N34
EBI1_D29 R29
EBI1_D30 R28
EBI1_D31 T26
IO_L4P_16
IO_L1P_16
IO_L14N_VREF_16
IO_L6N_16
IO_L8P_SRCC_16
IO_L3N_16
IO_L7P_16
IO_L8N_SRCC_16
IO_L19N_16
IO_L6N_SM11N_15
IO_L2P_SM8P_15
IO_L7N_16
IO_L16P_16
IO_L13N_16
IO_L12N_VRP_16
IO_L12P_VRN_16
IO_L11N_SRCC_16
IO_L11P_SRCC_16
IO_L10N_MRCC_16
IO_L10P_MRCC_16
IO_L9N_MRCC_16
IO_L9P_MRCC_16
IO_L2N_SM8N_15
IO_L6P_SM11P_15
IO_L1P_15
IO_L17N_15
IO_L14P_15
IO_L0P_15
IO_L16P_VRN_15
IO_L12N_SM13N_15
IO_L5N_SM10N_15
IO_L13N_SM14N_15
IO_L14N_VREF_15
IO_L16N_VRP_15
IO_L12P_SM13P_15
IO_L18N_15
IO_L18P_15
IO_L19N_15
IO_L13P_SM14P_15
IO_L15N_SM15N_15
BANK 16
XC6VLX240T-2FF1156I
IC2G
EBI1_D0 A17
EBI1_D1 D15
EBI1_D2 C15
EBI1_D3 B16
EBI1_D4 B15
EBI1_D5 D14
EBI1_D6 C14
EBI1_D7 A15
EBI1_D8 B14
EBI1_D9 D13
EBI1_D10 C13
EBI1_D11 E13
EBI1_D12 B13
EBI1_D13 E12
EBI1_D14 D12
EBI1_D15 C12
EBI1_NBS0/A0 F13
EBI1_NBS2/NWR2/A1 F14
EBI1_A2 F18
EBI1_A3 F15
EBI1_A4 E14
EBI1_A5 F17
EBI1_A6 F16
EBI1_A7 E17
EBI1_A8 E15
EBI1_A9 E16
EBI1_A10 D18
EBI1_A11 D17
EBI1_A12 C18
EBI1_A13 B18
EBI1_A14 A18
EBI1_A15 B17
EBI1_BA0/A16 C10
EBI1_BA1/A17 B10
EBI1_A18 C17
EBI1_DQM0 B11
EBI1_DQM1 D11
EBI1_DQS0 A11
EBI1_DQS1 E11
EBI1_RAS A12
EBI1_CAS C11
EBI1_SDWE F12
EBI1_SDA10 B9
EBI1_SDCKE B12
EBI1_SDCK A13
EBI1_NSDCK A14
EBI1_NCS0 A10
EBI1_NCS1/SDCS F10
EBI1_NRD/CFOE F11
EBI1_NWE/NWR0/CFWE C9
EBI1_NBS1/NWR1/CFIOR D9
EBI1_NBS3/NWR3/CFIOW A9
EBI1_NANDOE D10
EBI1_NANDWE E10
AT91SAM9G45-CU
GND
R25 10K
FBOOT_SEL
IC4A
SN74LVC1G32
R22 10K
R24 10K
R23 10K
NAND_RB
IC4B
SN74AHC1G32
C65 100nF
IC5
NAND_CLE D5
NAND_ALE C4
NAND_OE D4
NAND_WE C7
C6
R/B C8
WP C3
LOCK G5
CLE
ALE
RE
WE
CE
VCC
VSS
C69 100nF
C68 100nF
C67 100nF
C66 100nF
IO0 H4 EBI1_D0
IO1 J4 EBI1_D1
IO2 K4 EBI1_D2
IO3 K5 EBI1_D3
IO4 K6 EBI1_D4
IO5 J7 EBI1_D5
IO6 K7 EBI1_D6
IO7 J8 EBI1_D7
IO8 H3 EBI1_D8
IO9 J3 EBI1_D9
IO10 H5 EBI1_D10
IO11 J5 EBI1_D11
IO12 H6 EBI1_D12
IO13 G6 EBI1_D13
IO14 H7 EBI1_D14
IO15 G7 EBI1_D15
MT29F4G16ABBDAH4-ITD
IC1D
EBI1_A0 J30
EBI1_A1 H30
EBI1_A2 D32
EBI1_A3 G31
EBI1_A4 J27
EBI1_A5 E33
EBI1_A6 L28
EBI1_A7 D31
EBI1_A8 F30
EBI1_A9 E32
EBI1_A10 G32
EBI1_A11 H32
EBI1_A12 L26
EBI1_A13 C33
EBI1_A14 B32
EBI1_A15 B33
L30
L29
M33
N33
N29
N28
P32
N32
EBI1_A16 L25
EBI1_A17 L31
EBI1_A18 C32
EBI1_A19 M30
EBI1_A20 M28
N27
P30
P31
M27
M26
EBI1_NBS3 J34
EBI1_NCS0 H34
EBI1_NRD J31
EBI1_NWE M25
EBI1_NBS1 P29
EBI1_NWAIT R26
IO_L13P_16
IO_L5N_16
IO_L15N_16
IO_L5P_16
IO_L1N_16
IO_L2N_16
IO_L7P_SM12P_15
IO_L15P_16
IO_L3P_16
IO_L2P_16
IO_L17P_16
IO_L17N_16
IO_L18N_16
IO_L6P_16
IO_L0N_16
IO_L4N_VREF_16
IO_L11N_SRCC_15
IO_L11P_SRCC_15
IO_L10N_MRCC_15
IO_L10P_MRCC_15
IO_L9N_MRCC_15
IO_L9P_MRCC_15
IO_L8N_SRCC_15
IO_L8P_SRCC_15
IO_L18P_16
IO_L0N_15
IO_L0P_16
IO_L17P_15
IO_L7N_SM12N_15
IO_L5P_SM10P_15
IO_L4N_VREF_15
IO_L4P_15
IO_L3N_SM9N_15
IO_L3P_SM9P_15
IO_L16N_16
IO_L14P_16
IO_L19P_16
IO_L1N_15
IO_L19P_15
IO_L15P_SM15P_15
BANK 15
XC6VLX240T-2FF1156I
PCK0
ARM_PCK0
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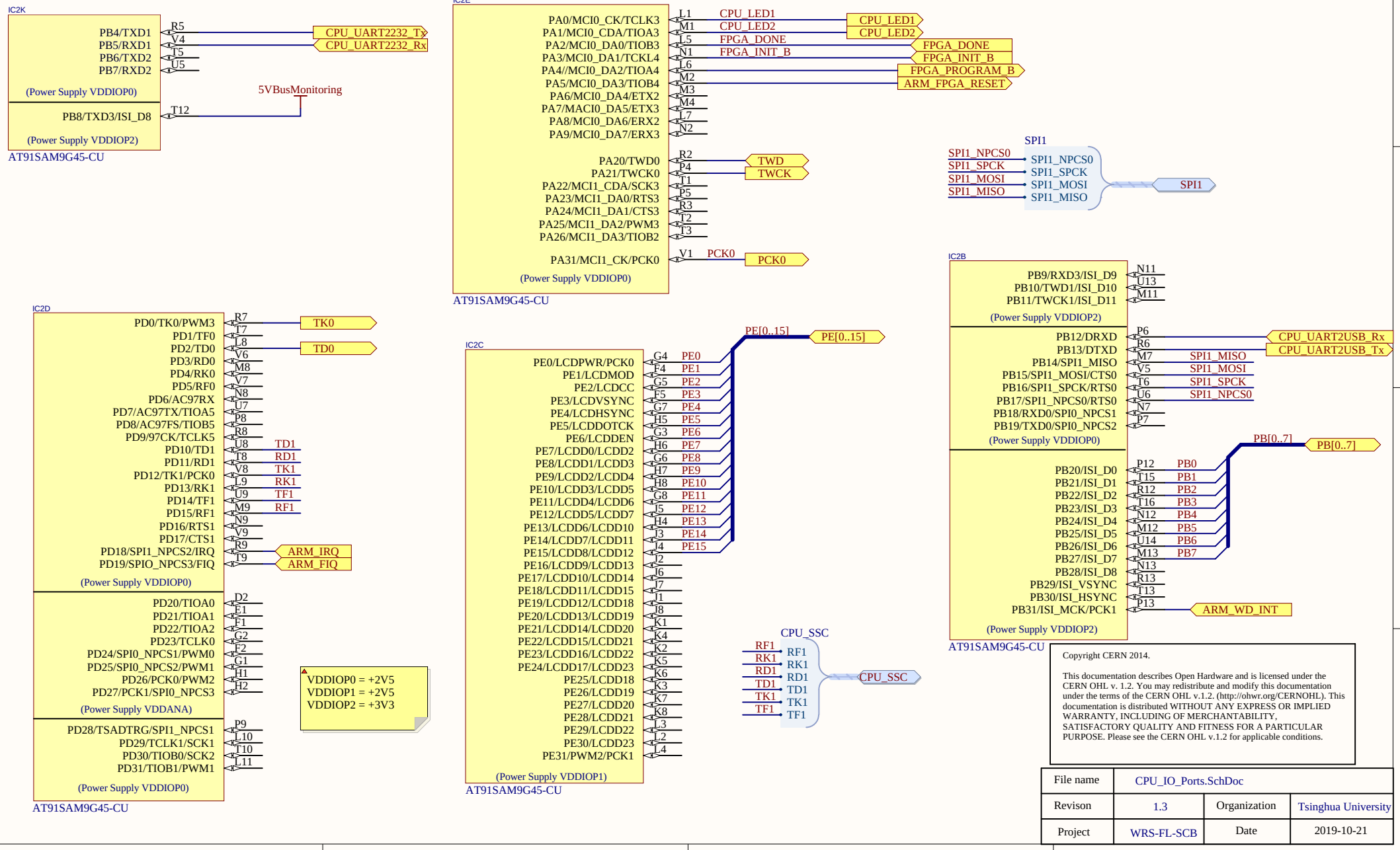
File name CPU_EBI1_FPGA_Memory.SchDoc
Revison 1.3
Organization Tsinghua University
Project WRS-FL-SCB
Date 2019-10-21


IC2K
PB4/TXD1
PB5/RXD1
PB6/TXD2
PB7/RXD2
(Power Supply VDDIOP0)
PB8/TXD3/ISI_D8
(Power Supply VDDIOP2)
AT91SAM9G45-CU
R5
V4
T5
U5
T12
CPU_UART2232_Tx
CPU_UART2232_Rx
5VBusMonitoring
IC2E
PA0/MCI0_CK/TCLK3
PA1/MCI0_CDA/TIOA3
PA2/MCI0_DA0/TIOB3
PA3/MCI0_DA1/TCKL4
PA4//MCI0_DA2/TIOA4
PA5/MCI0_DA3/TIOB4
PA6/MCI0_DA4/ETX2
PA7/MACI0_DA5/ETX3
PA8/MCI0_DA6/ERX2
PA9/MCI0_DA7/ERX3
PA20/TWD0
PA21/TWCK0
PA22/MCI1_CDA/SCK3
PA23/MCI1_DA0/RTS3
PA24/MCI1_DA1/CTS3
PA25/MCI1_DA2/PWM3
PA26/MCI1_DA3/TIOB2
PA31/MCI1_CK/PCK0
(Power Supply VDDIOP0)
AT91SAM9G45-CU
L1
M1
L5
N1
L6
M2
M3
M4
L7
N2
R2
P4
T1
P5
R3
T2
T3
V1
CPU_LED1
CPU_LED2
FPGA_DONE
FPGA_INIT_B
FPGA_PROGRAM_B
ARM_FPGA_RESET
TWD
TWCK
PCK0
SPI1
SPI1_NPCS0
SPI1_SPCK
SPI1_MOSI
SPI1_MISO
IC2B
PB9/RXD3/ISI_D9
PB10/TWD1/ISI_D10
PB11/TWCK1/ISI_D11
(Power Supply VDDIOP2)
PB12/DRXD
PB13/DTXD
PB14/SPI1_MISO
PB15/SPI1_MOSI/CTS0
PB16/SPI1_SPCK/RTS0
PB17/SPI1_NPCS0/RTS0
PB18/RXD0/SPI0_NPCS1
PB19/TXD0/SPI0_NPCS2
(Power Supply VDDIOP0)
PB20/ISI_D0
PB21/ISI_D1
PB22/ISI_D2
PB23/ISI_D3
PB24/ISI_D4
PB25/ISI_D5
PB26/ISI_D6
PB27/ISI_D7
PB28/ISI_D8
PB29/ISI_VSYNC
PB30/ISI_HSYNC
PB31/ISI_MCK/PCK1
(Power Supply VDDIOP2)
AT91SAM9G45-CU
N11
U13
M11
P6
R6
M7
V5
T6
U6
N7
P7
P12
T15
R12
T16
N12
M12
U14
M13
N13
R13
T13
P13
PB[0..7]
CPU_UART2USB_Rx
CPU_UART2USB_Tx
SPI1_MISO
SPI1_MOSI
SPI1_SPCK
SPI1_NPCS0
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
ARM_WD_INT
IC2D
PD0/TK0/PWM3
PD1/TF0
PD2/TD0
PD3/RD0
PD4/RK0
PD5/RF0
PD6/AC97RX
PD7/AC97TX/TIOA5
PD8/AC97FS/TIOB5
PD9/97CK/TCLK5
PD10/TD1
PD11/RD1
PD12/TK1/PCK0
PD13/RK1
PD14/TF1
PD15/RF1
PD16/RTS1
PD17/CTS1
PD18/SPI1_NPCS2/IRQ
PD19/SPIO_NPCS3/FIQ
(Power Supply VDDIOP0)
PD20/TIOA0
PD21/TIOA1
PD22/TIOA2
PD23/TCLK0
PD24/SPI0_NPCS1/PWM0
PD25/SPI0_NPCS2/PWM1
PD26/PCK0/PWM2
PD27/PCK1/SPI0_NPCS3
(Power Supply VDDANA)
PD28/TSADTRG/SPI1_NPCS1
PD29/TCLK1/SCK1
PD30/TIOB0/SCK2
PD31/TIOB1/PWM1
(Power Supply VDDIOP0)
AT91SAM9G45-CU
R7
T7
L8
V6
M8
V7
N8
U7
P8
R8
U8
T8
V8
L9
U9
M9
N9
V9
R9
T9
D2
E1
F1
G2
F2
G1
H1
H2
P9
L10
T10
L11
TK0
TD0
TD1
RD1
TK1
RK1
TF1
RF1
ARM_IRQ
ARM_FIQ
VDDIOP0 = +2V5
VDDIOP1 = +2V5
VDDIOP2 = +3V3
IC2C
PE0/LCDPWR/PCK0
PE1/LCDMOD
PE2/LCDCC
PE3/LCDVSYNC
PE4/LCDHSYNC
PE5/LCDDOTCK
PE6/LCDDEN
PE7/LCDD0/LCDD2
PE8/LCDD1/LCDD3
PE9/LCDD2/LCDD4
PE10/LCDD3/LCDD5
PE11/LCDD4/LCDD6
PE12/LCDD5/LCDD7
PE13/LCDD6/LCDD10
PE14/LCDD7/LCDD11
PE15/LCDD8/LCDD12
PE16/LCDD9/LCDD13
PE17/LCDD10/LCDD14
PE18/LCDD11/LCDD15
PE19/LCDD12/LCDD18
PE20/LCDD13/LCDD19
PE21/LCDD14/LCDD20
PE22/LCDD15/LCDD21
PE23/LCDD16/LCDD22
PE24/LCDD17/LCDD23
PE25/LCDD18
PE26/LCDD19
PE27/LCDD20
PE28/LCDD21
PE29/LCDD22
PE30/LCDD23
PE31/PWM2/PCK1
(Power Supply VDDIOP1)
AT91SAM9G45-CU
G4
F4
G5
F5
G7
H5
G3
H6
G6
H7
H8
G8
J5
H4
J3
J4
J2
J6
J7
J1
J8
K1
K4
K2
K5
K6
K3
K7
K8
J3
L2
L4
PE0
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PE8
PE9
PE10
PE11
PE12
PE13
PE14
PE15
PE[0..15]
CPU_SSC
RF1
RK1
RD1
TD1
TK1
TF1
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File name
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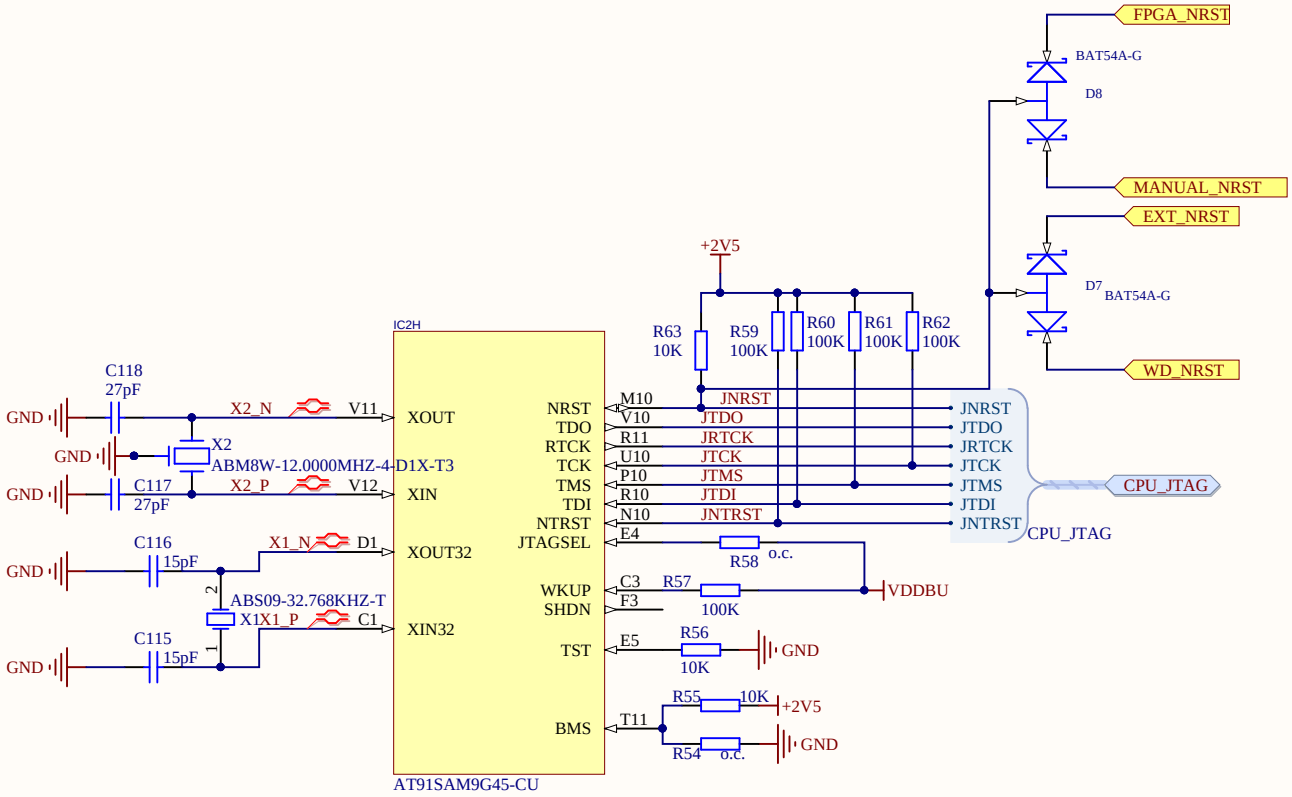
Revison
1.3
Organization
Tsinghua University
Project
WRS-FL-SCB
Date
2019-10-21



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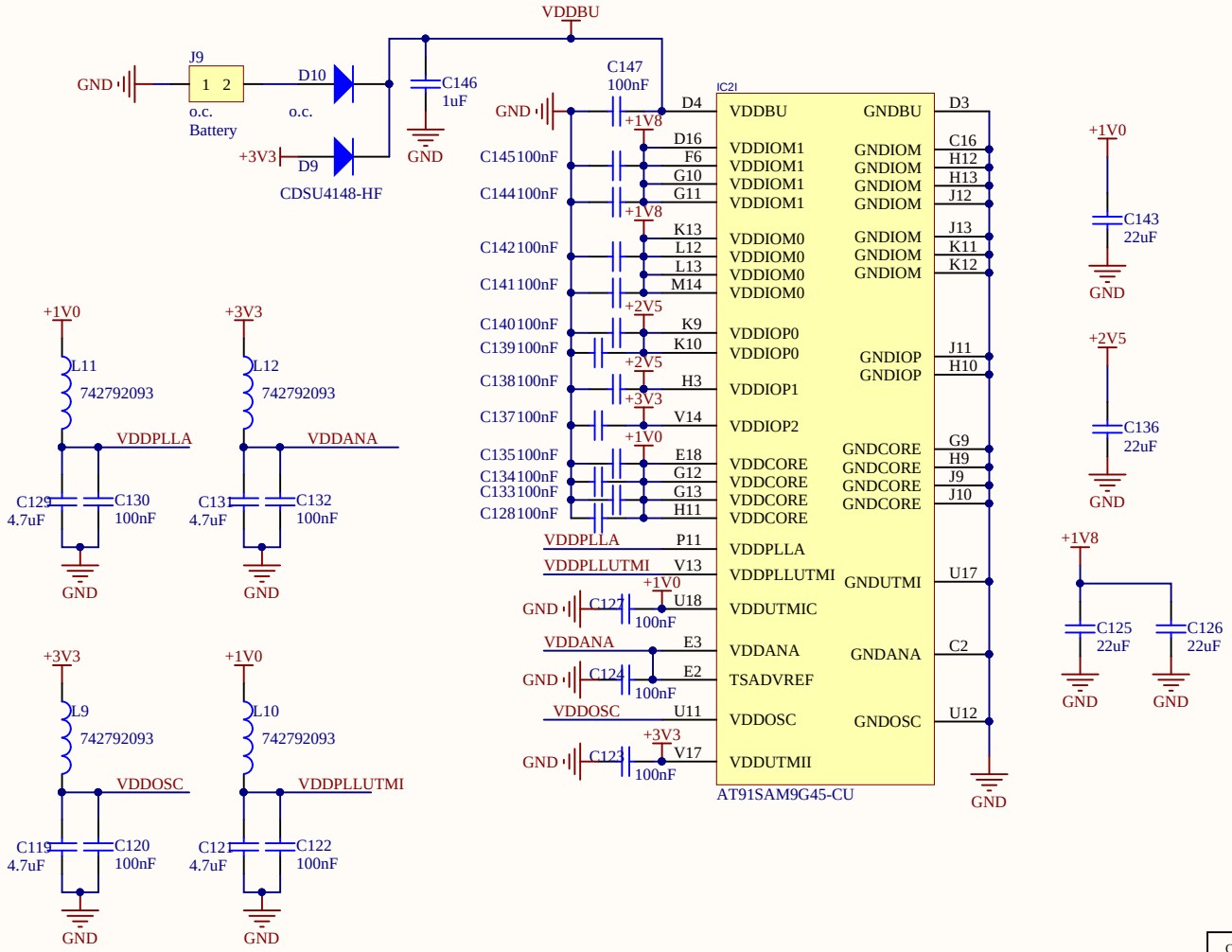
Revison	1.3	Organization	Tsinghua University
Project	White Rabbit	Date	2019-10-21



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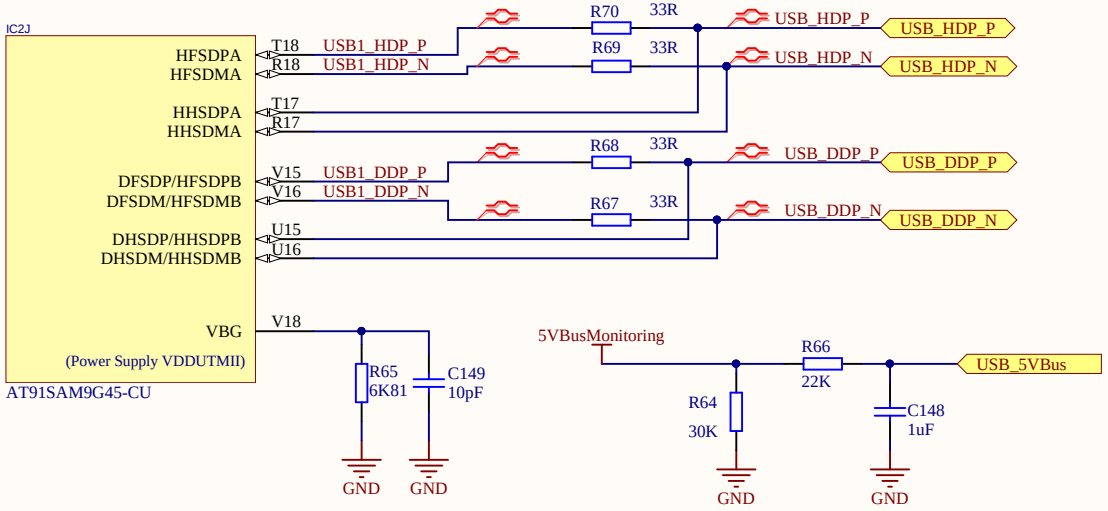
Revison	1.3	Organization	Tsinghua University
Project	White Rabbit	Date	2019-10-21



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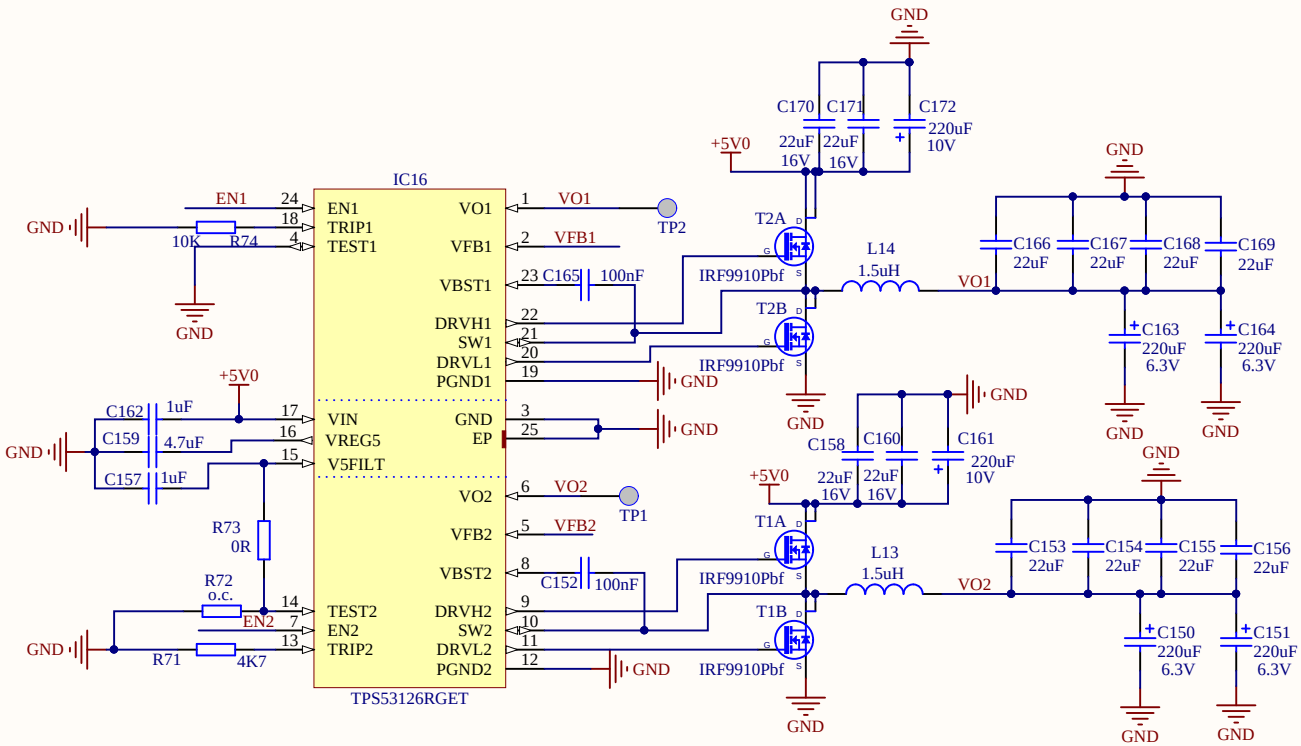
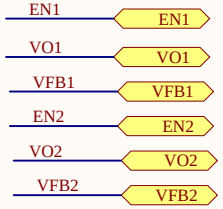
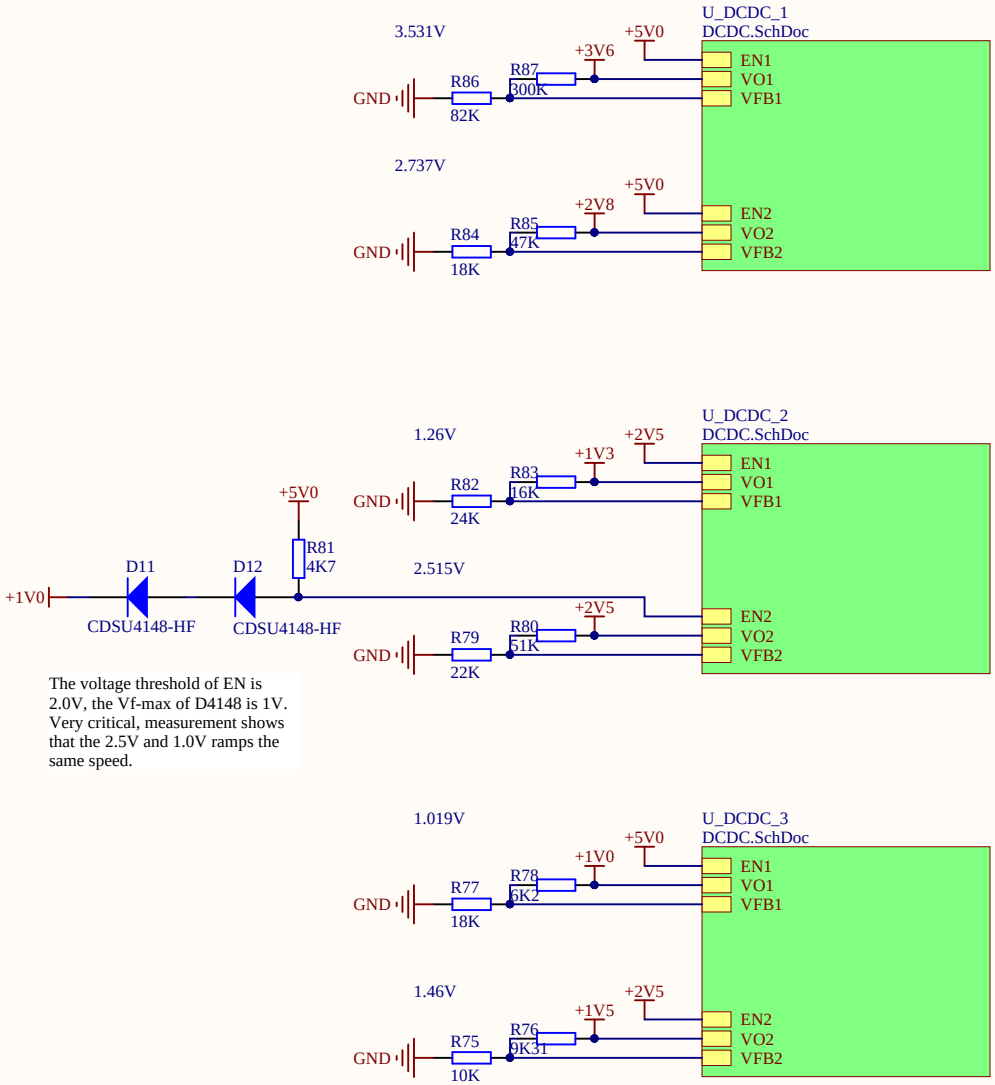
Revison	1.3	Organization	Tsinghua University
Project	White Rabbit	Date	2019-10-21





File name	DCDC.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21

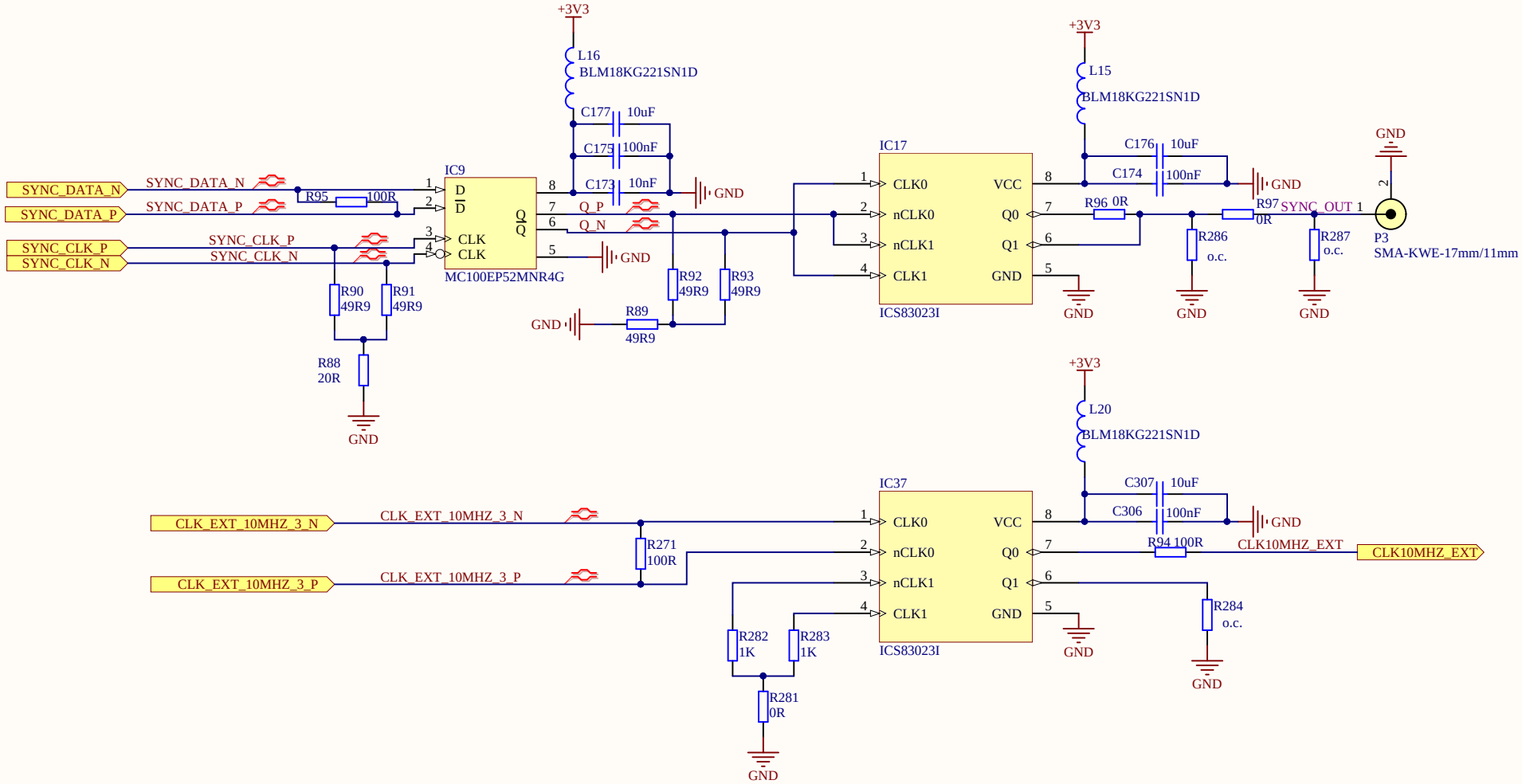


The voltage threshold of EN is 2.0V, the Vf-max of D4148 is 1V. Very critical, measurement shows that the 2.5V and 1.0V ramps the same speed.

$$R1 = \left(\frac{Vo1}{0.765 + \frac{VFB1_{(ripple)}}{2}} - 1 \right) \times R2 \qquad \text{(TEST2=GND)}$$

$$R1 = \left(\frac{Vo1}{0.758 + \frac{VFB1_{(ripple)}}{2}} - 1 \right) \times R2 \qquad \text{(TEST2 = V5FILT)}$$

File name	DCDC_ALL.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



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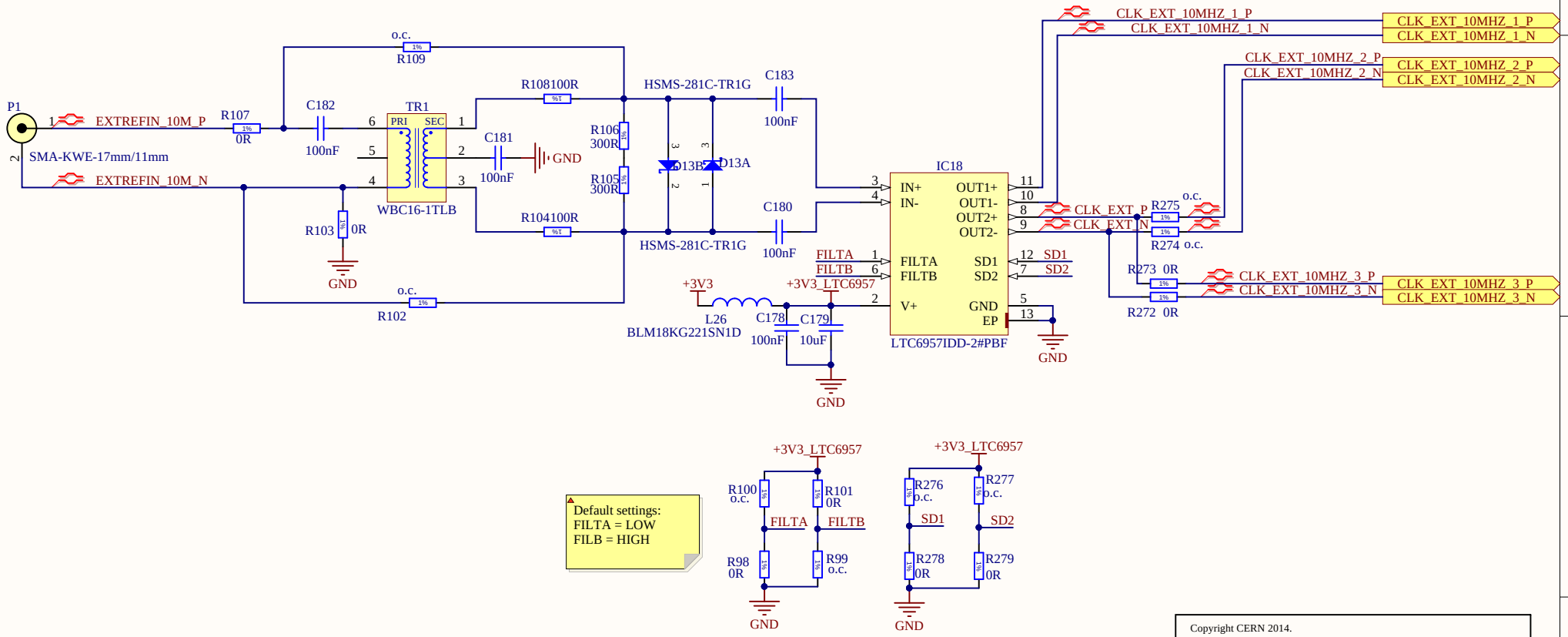
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



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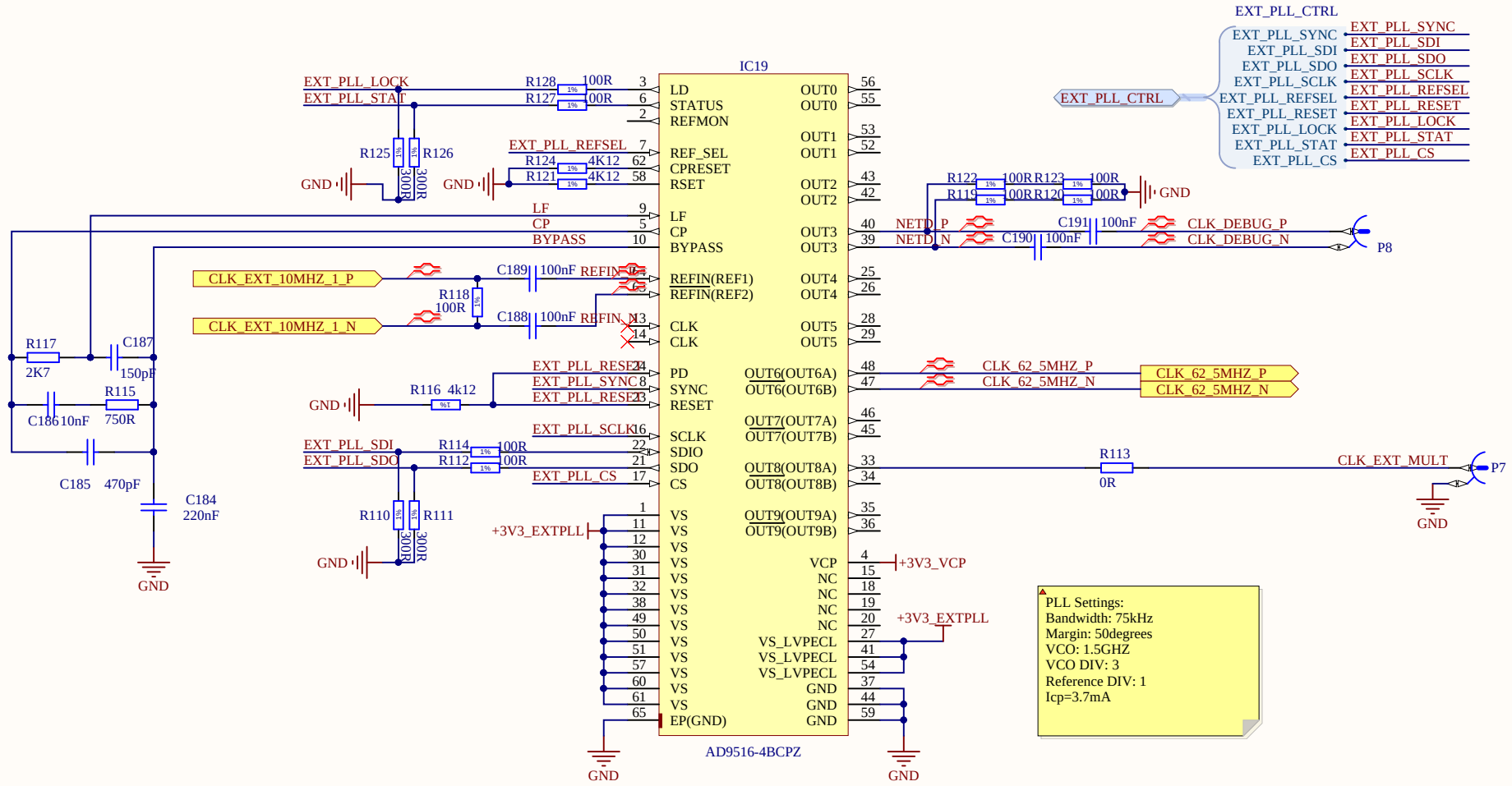
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



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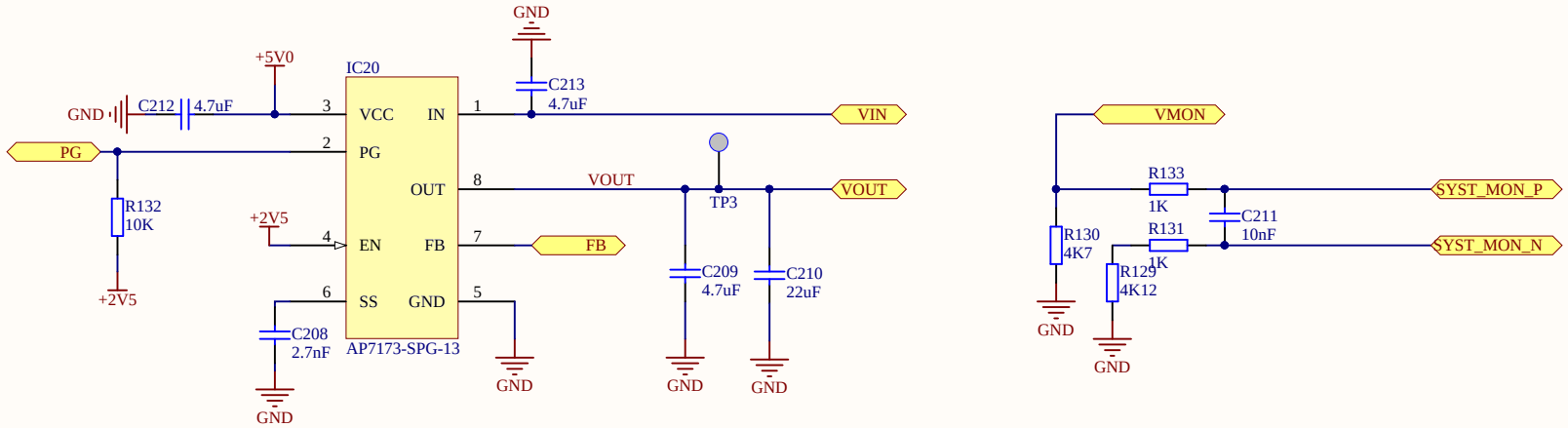
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21


GND
+5V0
IC20
C213
4.7uF
GND
C212
4.7uF
3
VCC
IN
1
VIN
PG
2
PG
OUT
8
VOUT
VOUT
TP3
R132
10K
+2V5
4
EN
FB
7
FB
C209
4.7uF
C210
22uF
6
SS
GND
5
C208
2.7nF
AP7173-SPG-13
GND
GND
GND
GND
VMON
R133
1K
SYST_MON_P
C211
10nF
R130
4K7
R131
1K
SYST_MON_N
R129
4K12
GND
GND

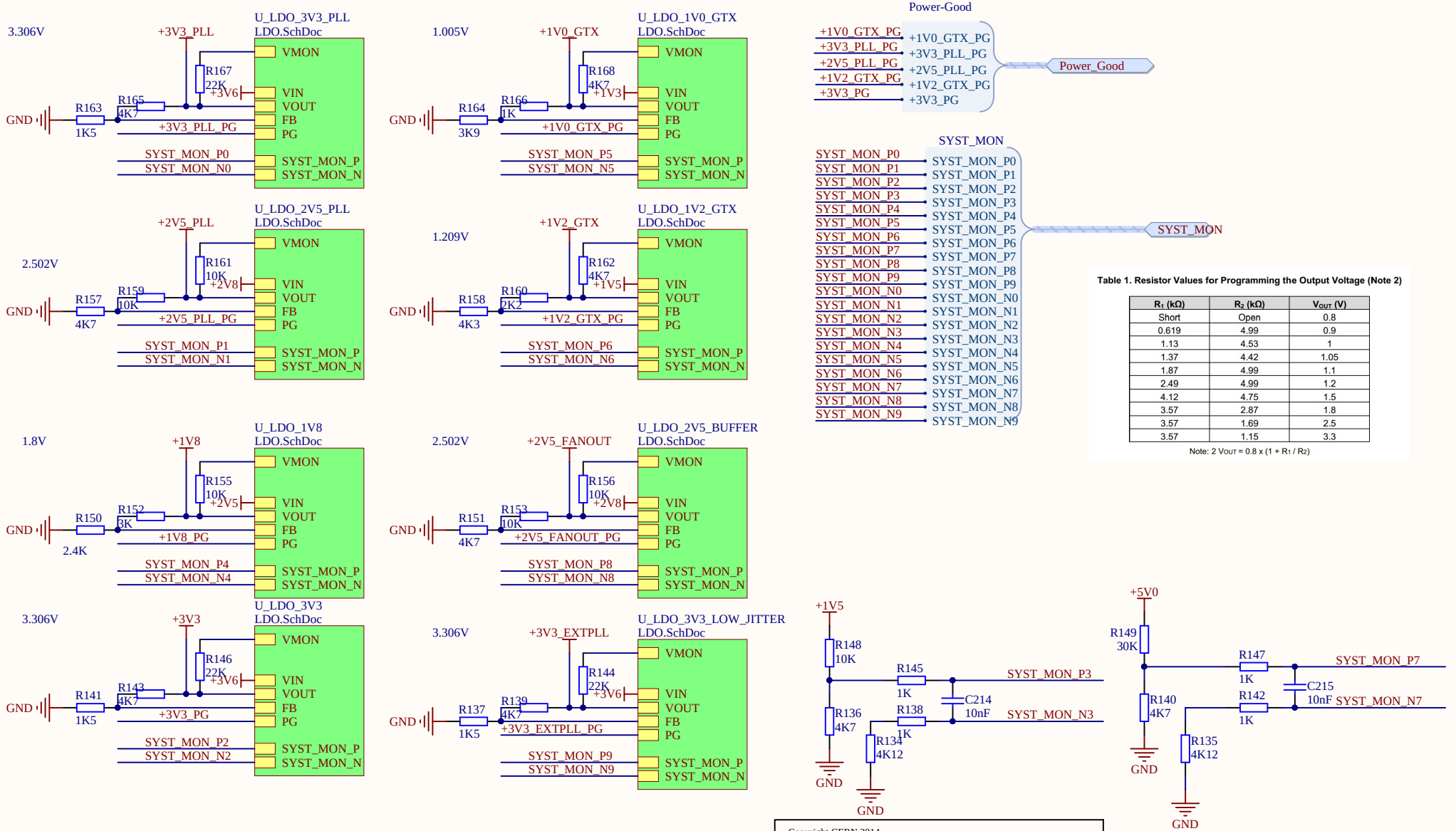
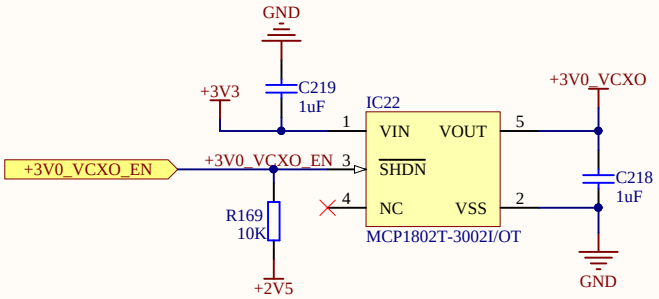


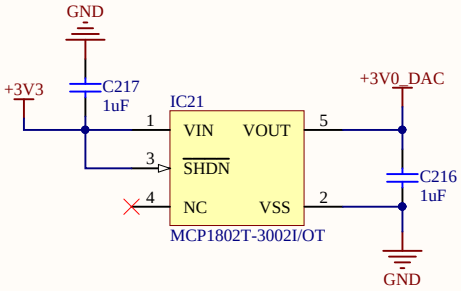
Table 1. Resistor Values for Programming the Output Voltage (Note 2)

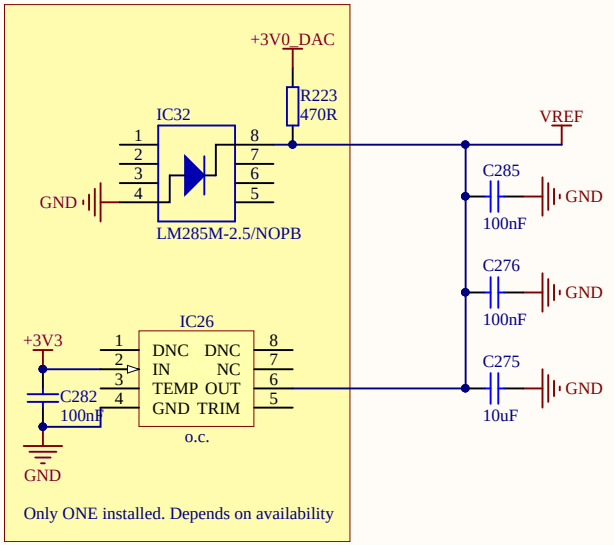
R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

Note: 2 $V_{OUT} = 0.8 \times (1 + R_1 / R_2)$

File name	LDO_ALL.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21







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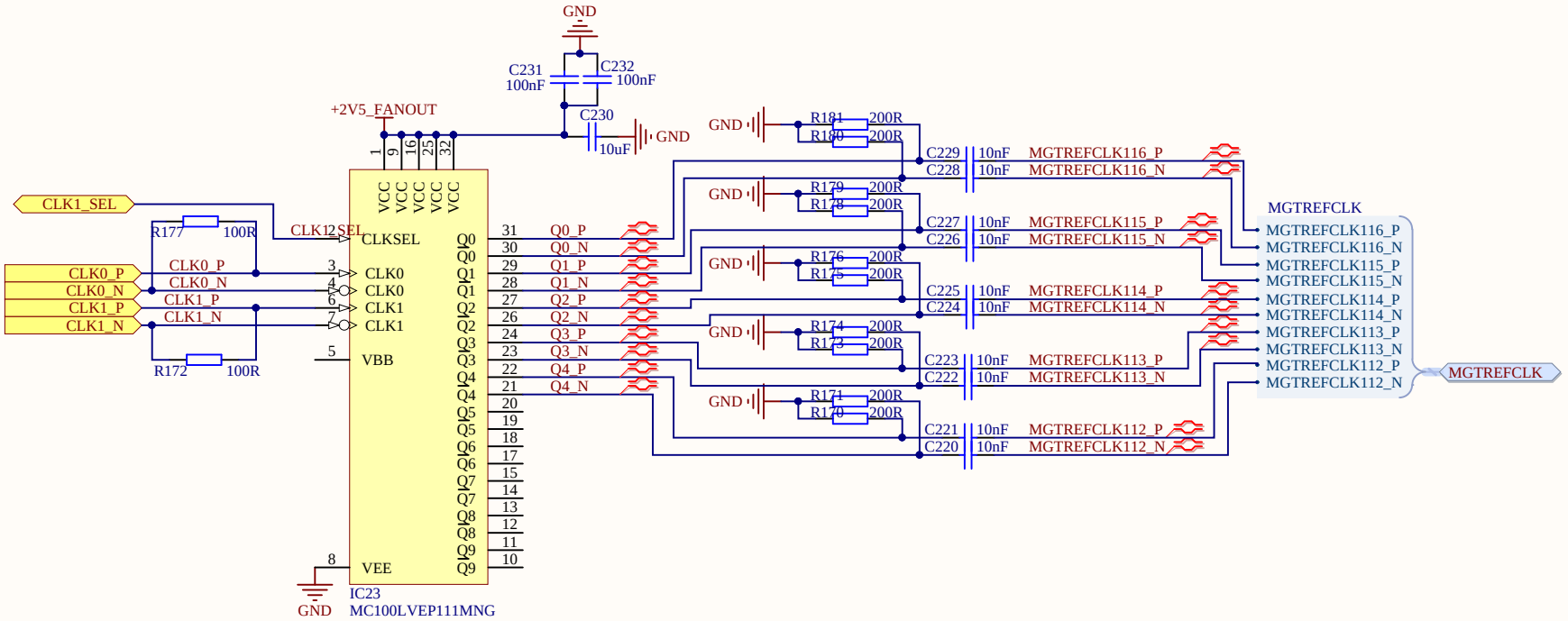
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



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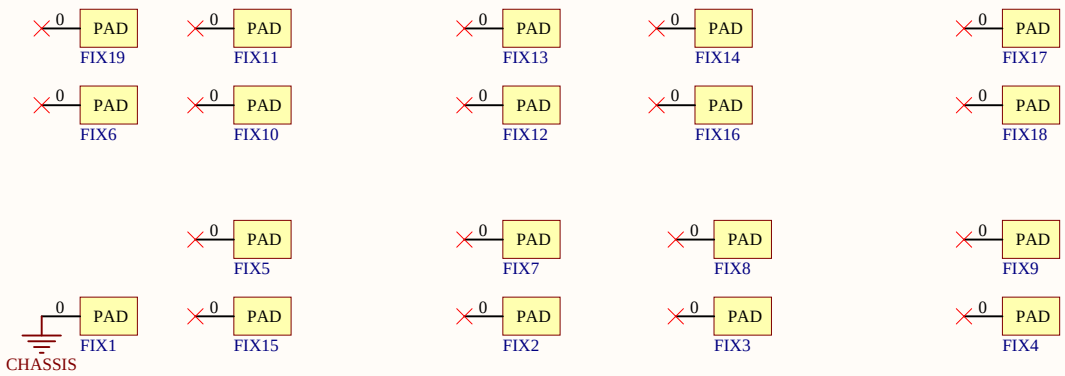
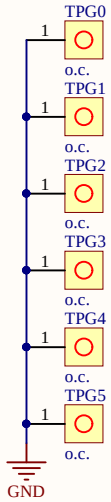
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21

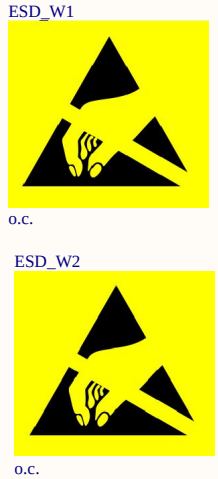


FFIX holes

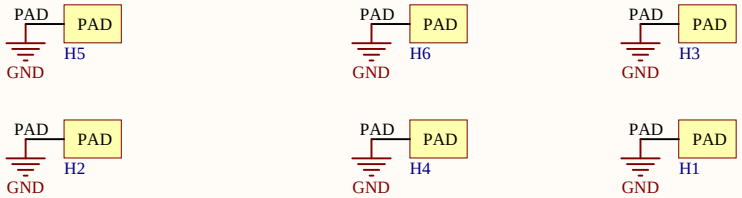


GND test point

Logo

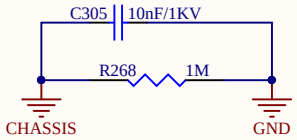


ESD warning drawing



Thermal PAD for the PCB

Scare Fiducial Target,



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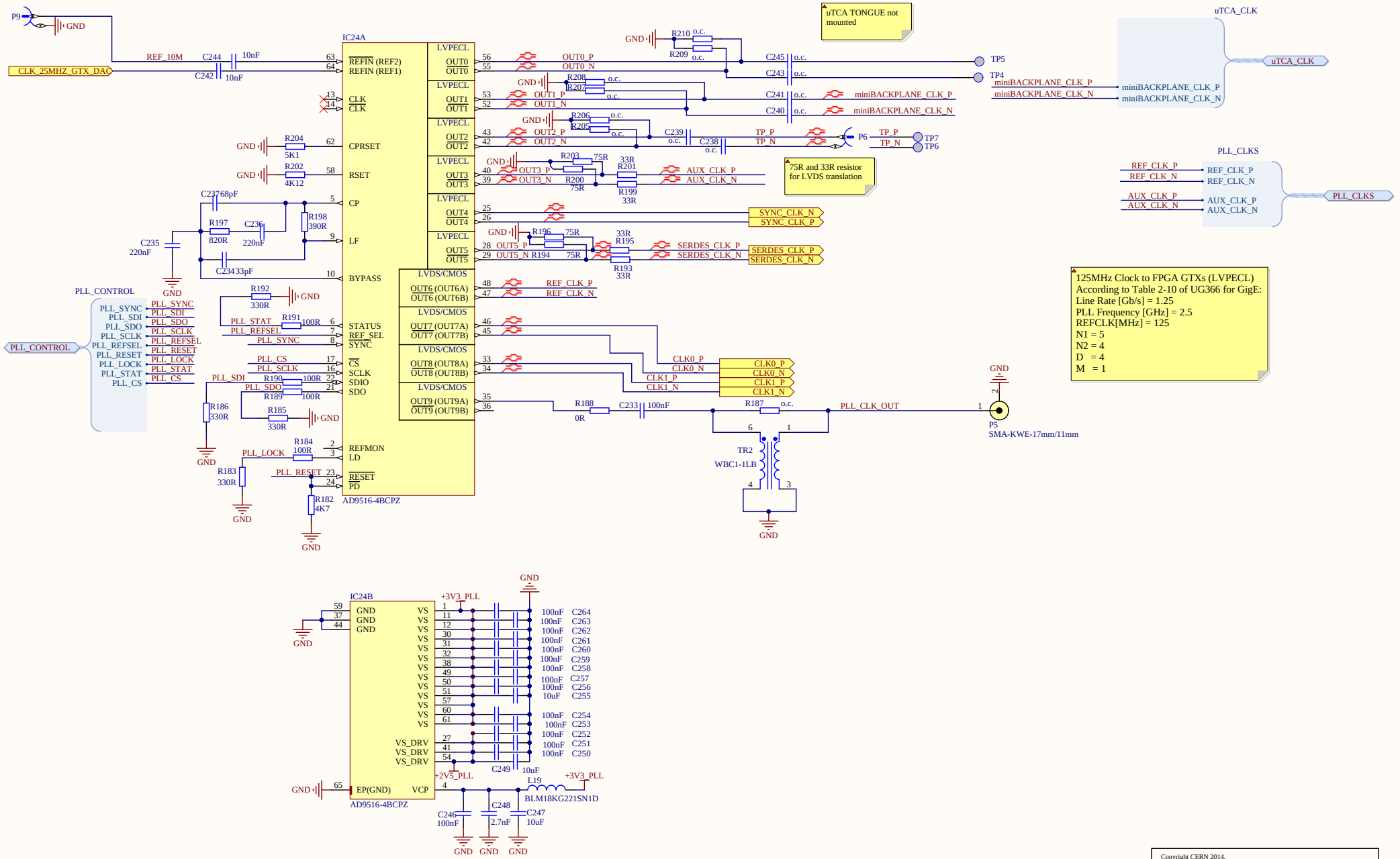
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



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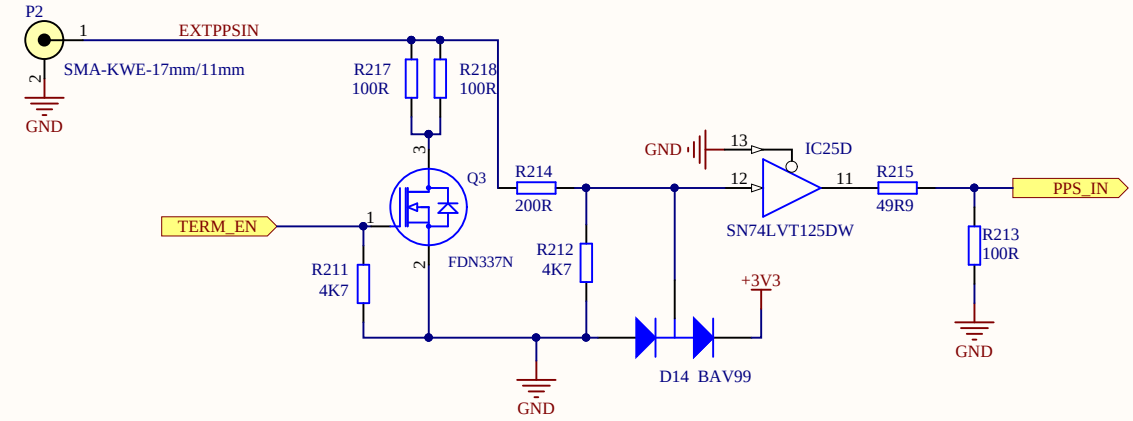
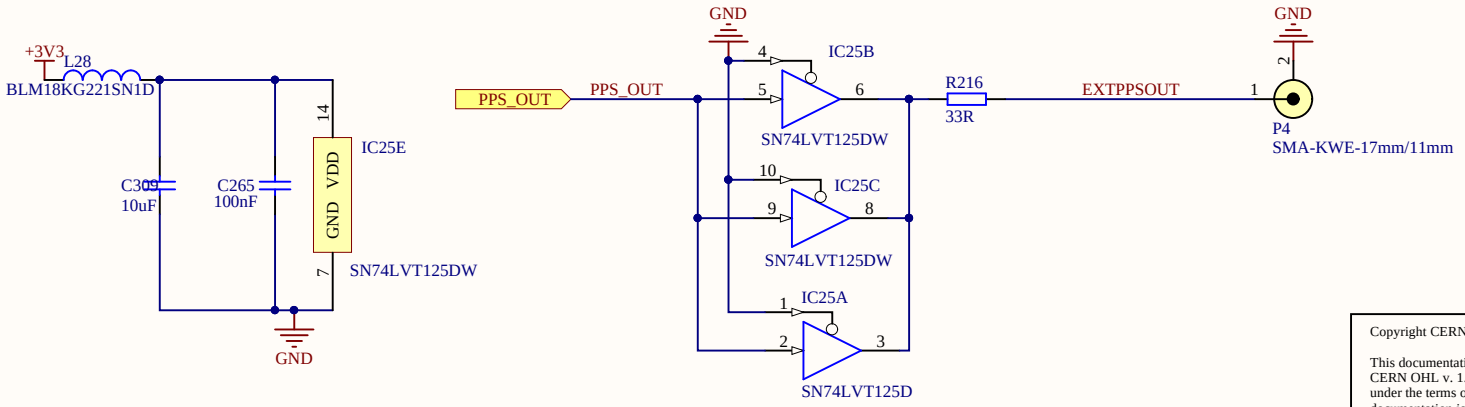
File name	PLL.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21





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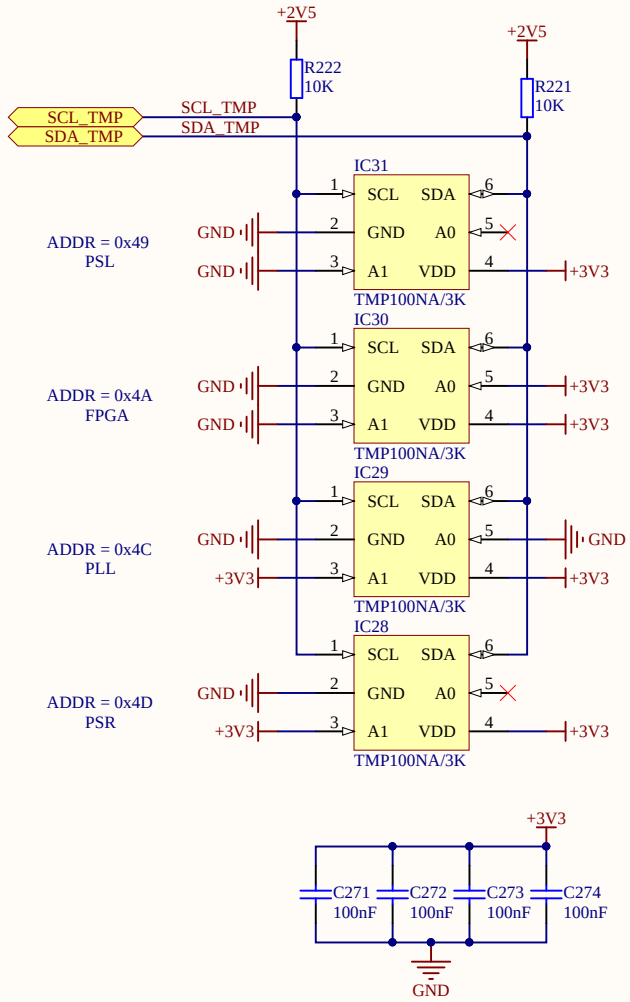
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



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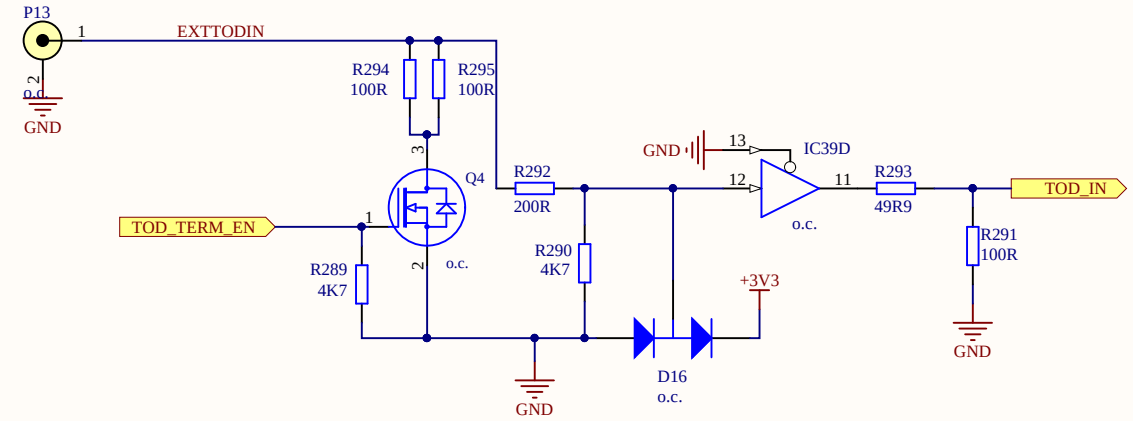
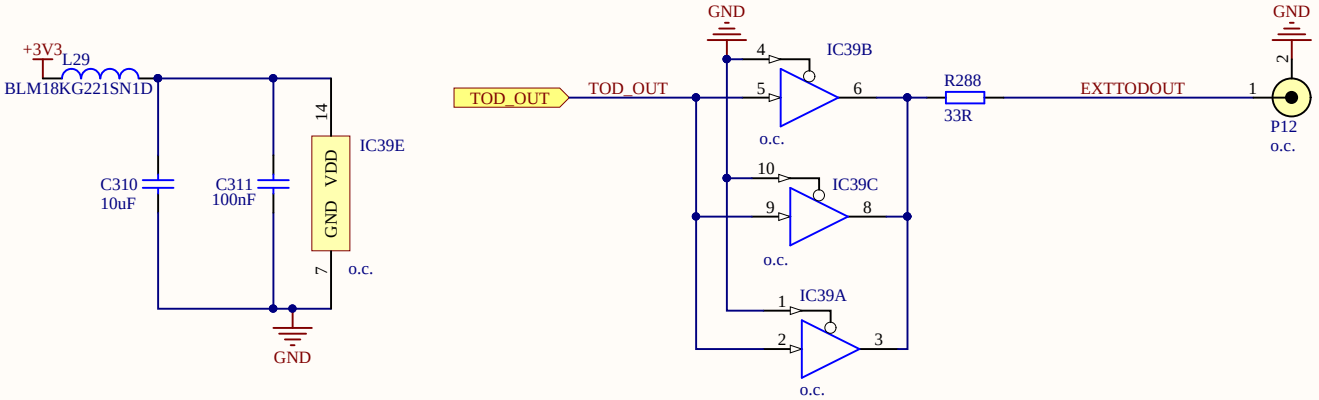
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21





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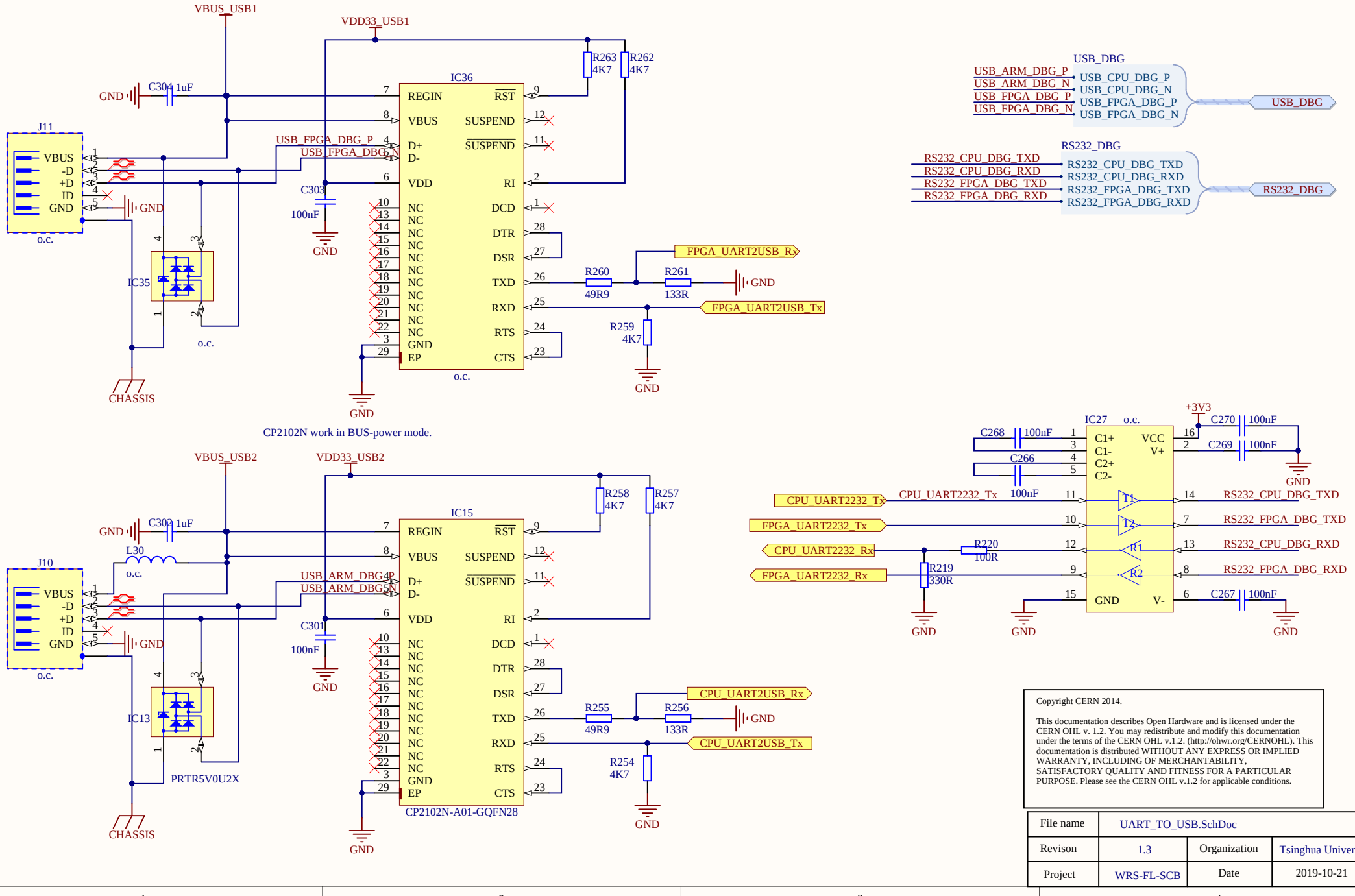
Revison	*	Organization	*
Project	White Rabbit	Date	2019-10-21



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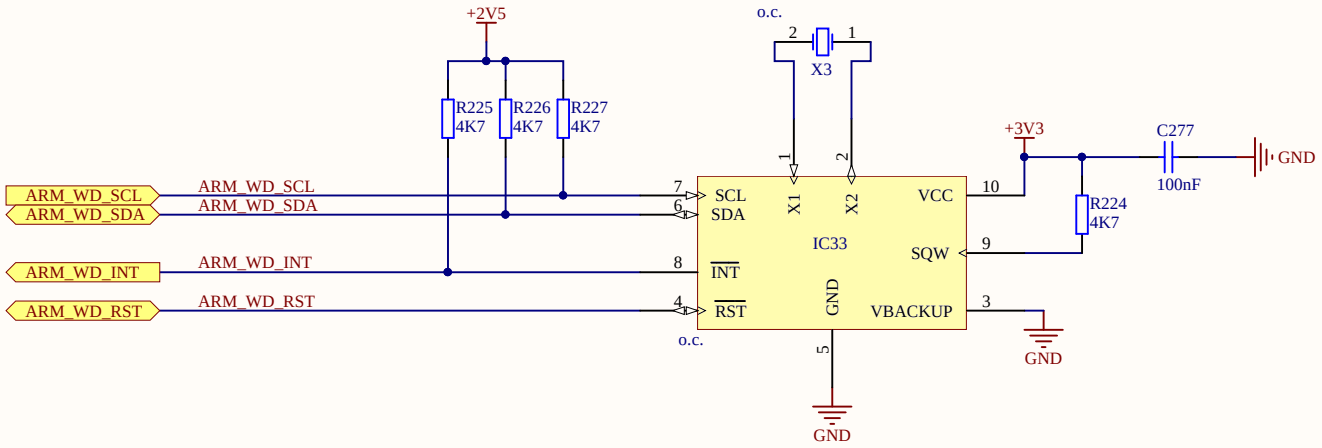
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21



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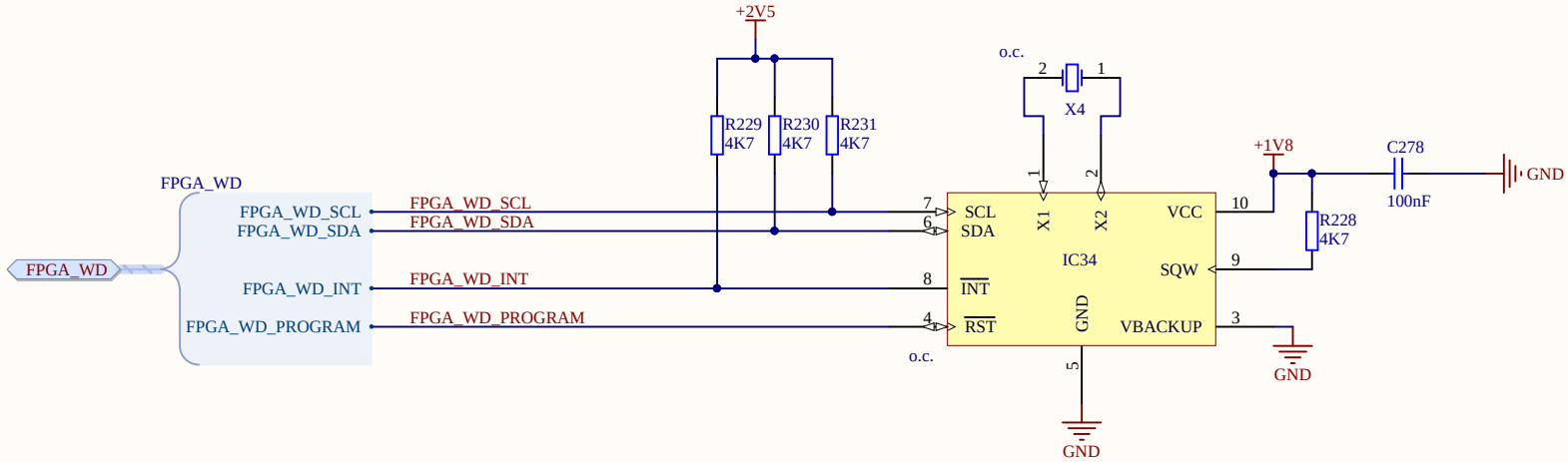
Revison	1.3	Organization	Tsinghua University
Project	White Rabbit	Date	2019-10-21



File name	WDT_FPGA.SchDoc		
Revison	1.3	Organization	Tsinghua University
Project	WRS-FL-SCB	Date	2019-10-21