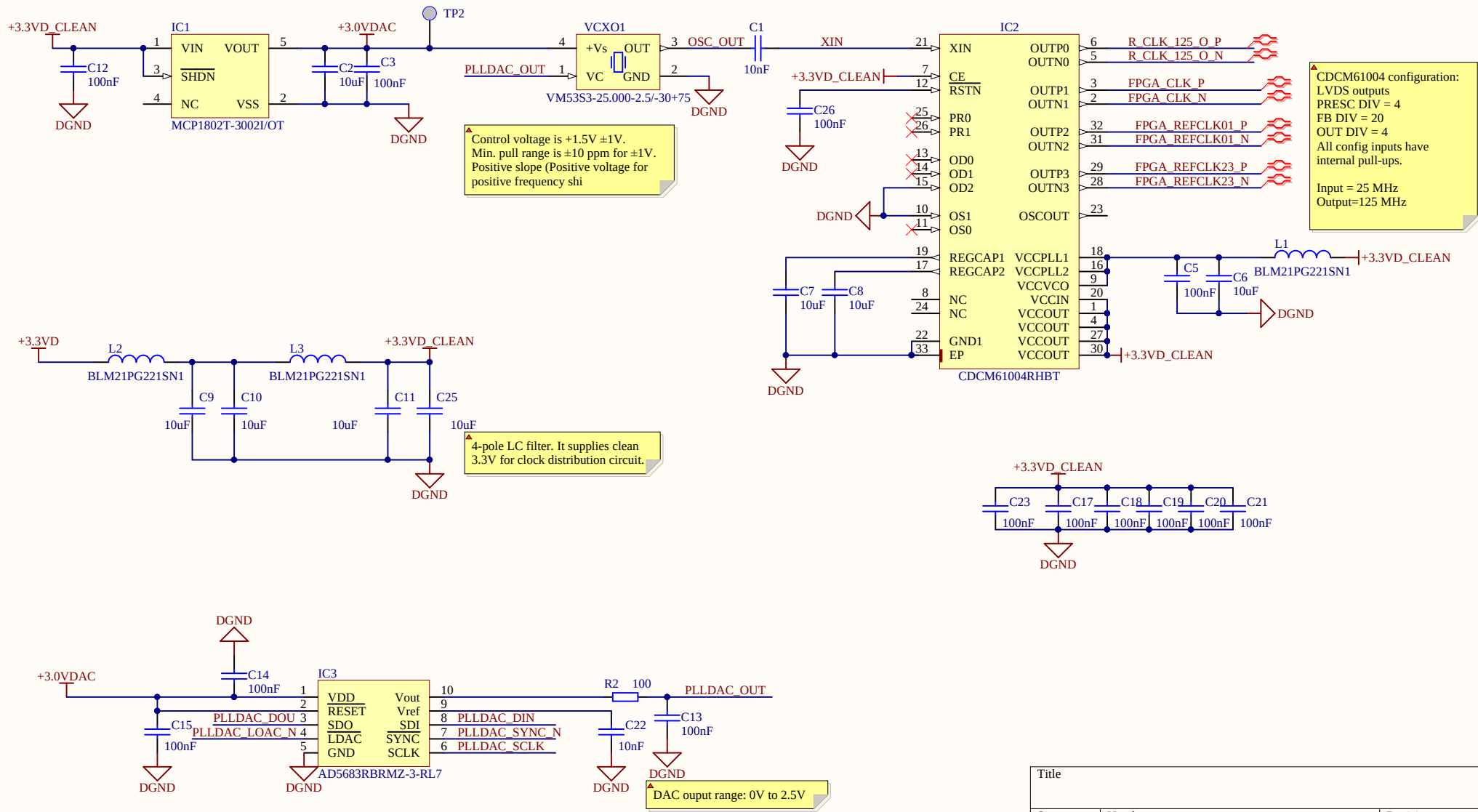
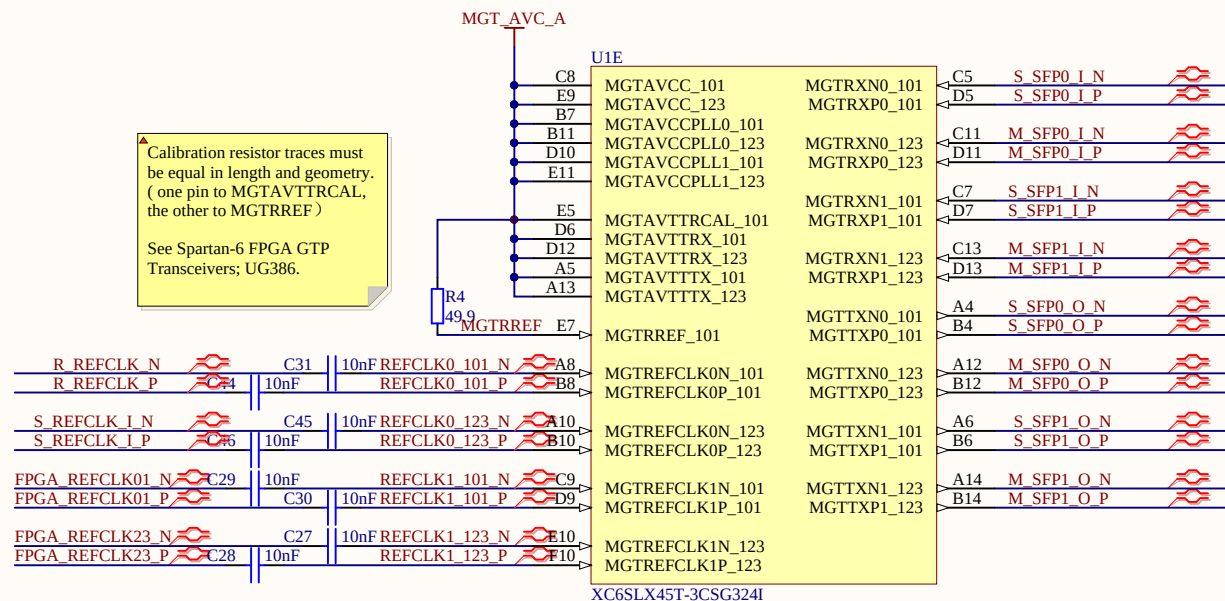




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▲ Calibration resistor traces must be equal in length and geometry. (one pin to MGTAVTTRCAL, the other to MGTTRREF)

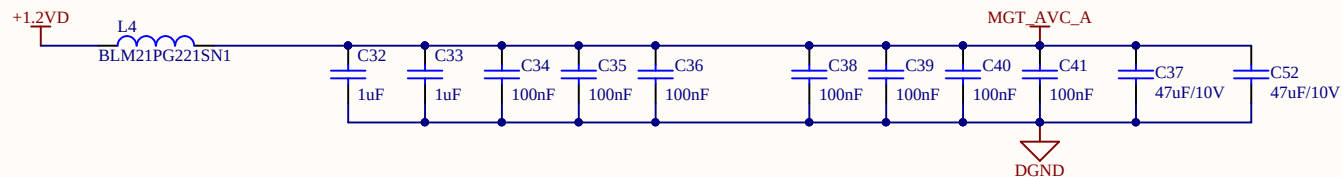
See Spartan-6 FPGA GTP Transceivers; UG386.



▲ HOW to Connect CLK when used all 4 GTPs???

▲ Power: GTPs power plane, and signal plane should be separated by a ground plane from any signal passing close.

The capacitor bank recommended for decoupling is described in: Xilinx user guide Spartan-6 FPGA GTP Transceivers (ug386.pdf). Chapter 5 Board Design Guidelines. Check Table 5-2: Recommended Minimum Decoupling for Spartan-6 FPGA GTPA1_DUAL Tiles and Figure 5-11: Stackup for GTP Power and Signal Layers.

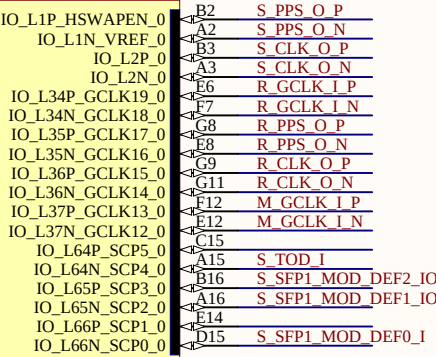


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Bank 0 Supports differential output

U1A

BANK 0

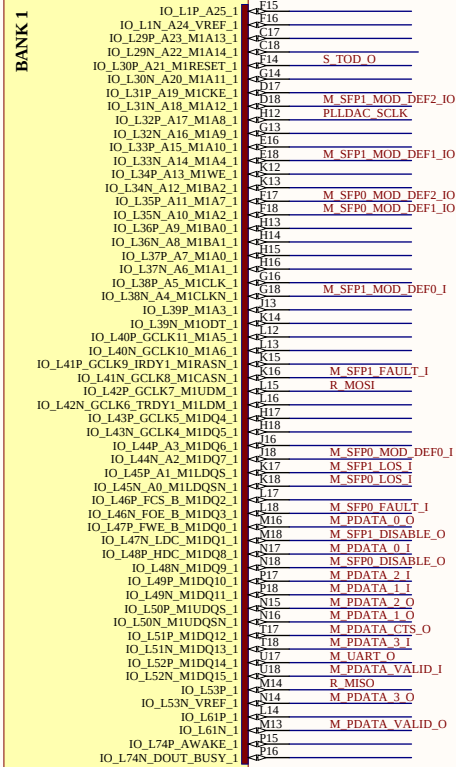


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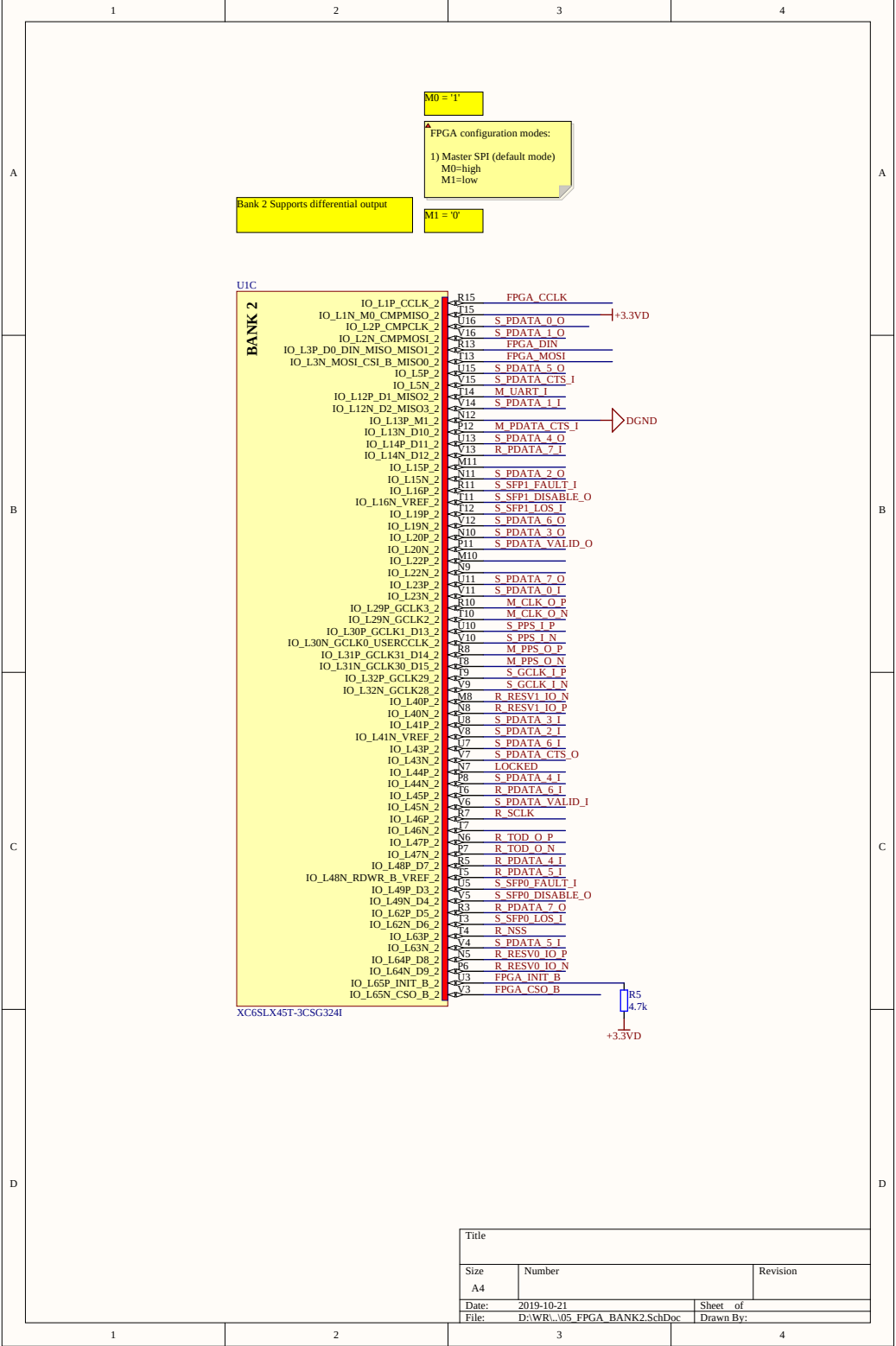
Bank 1 DOESN'T Supports differential output

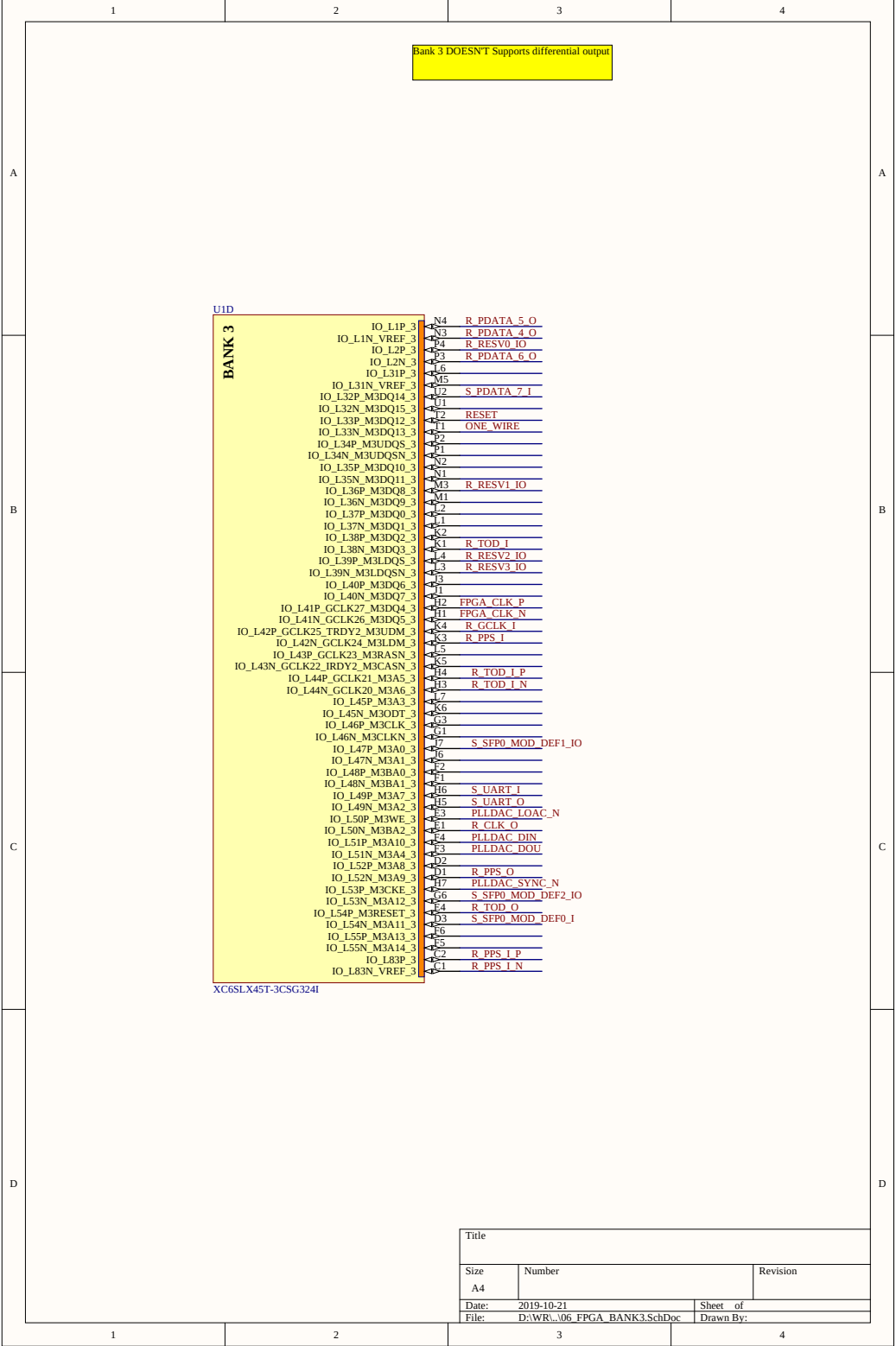
U1B

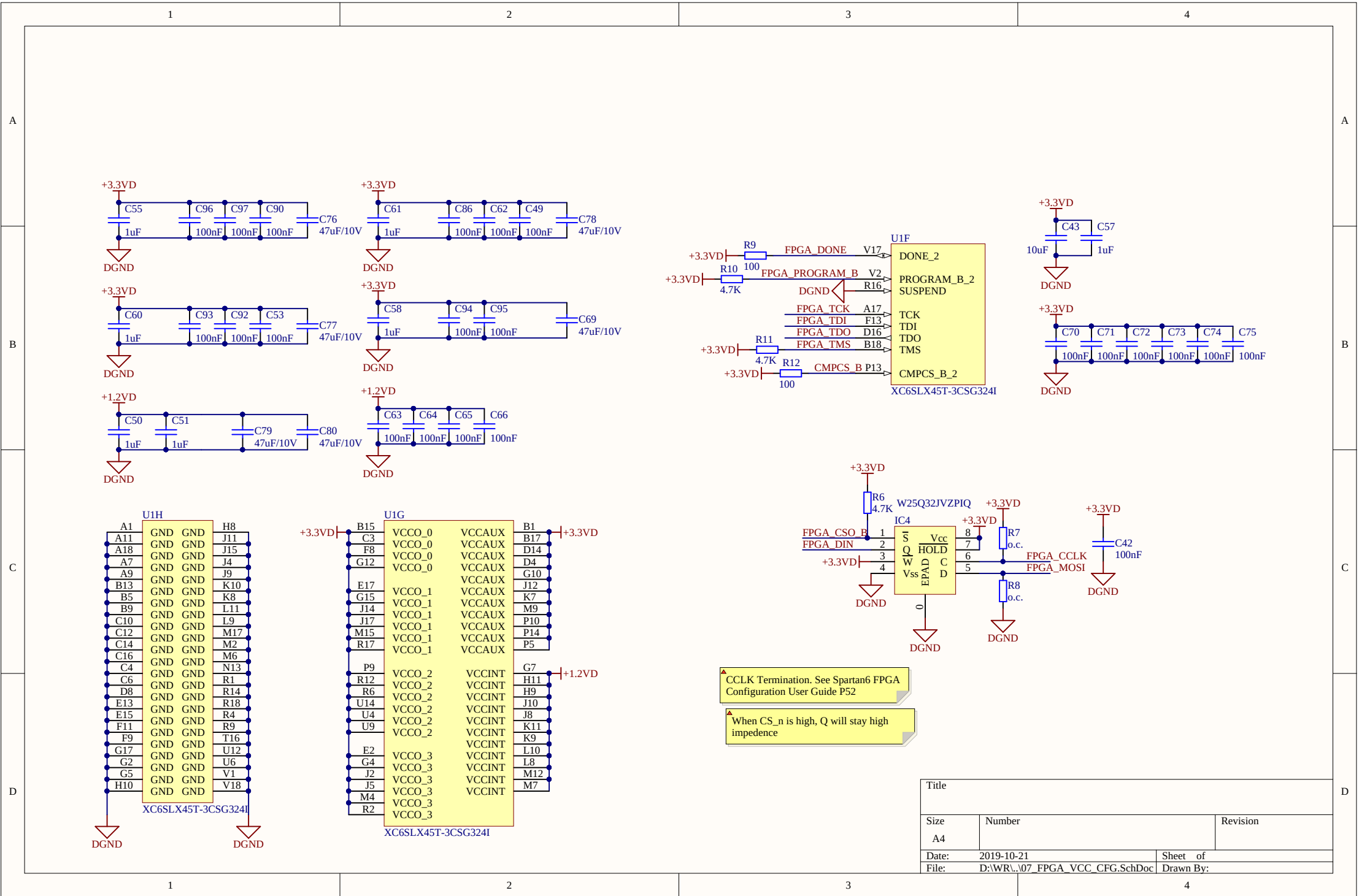


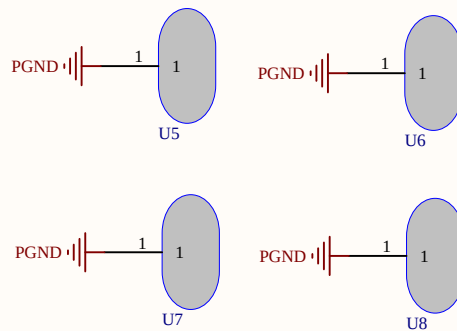
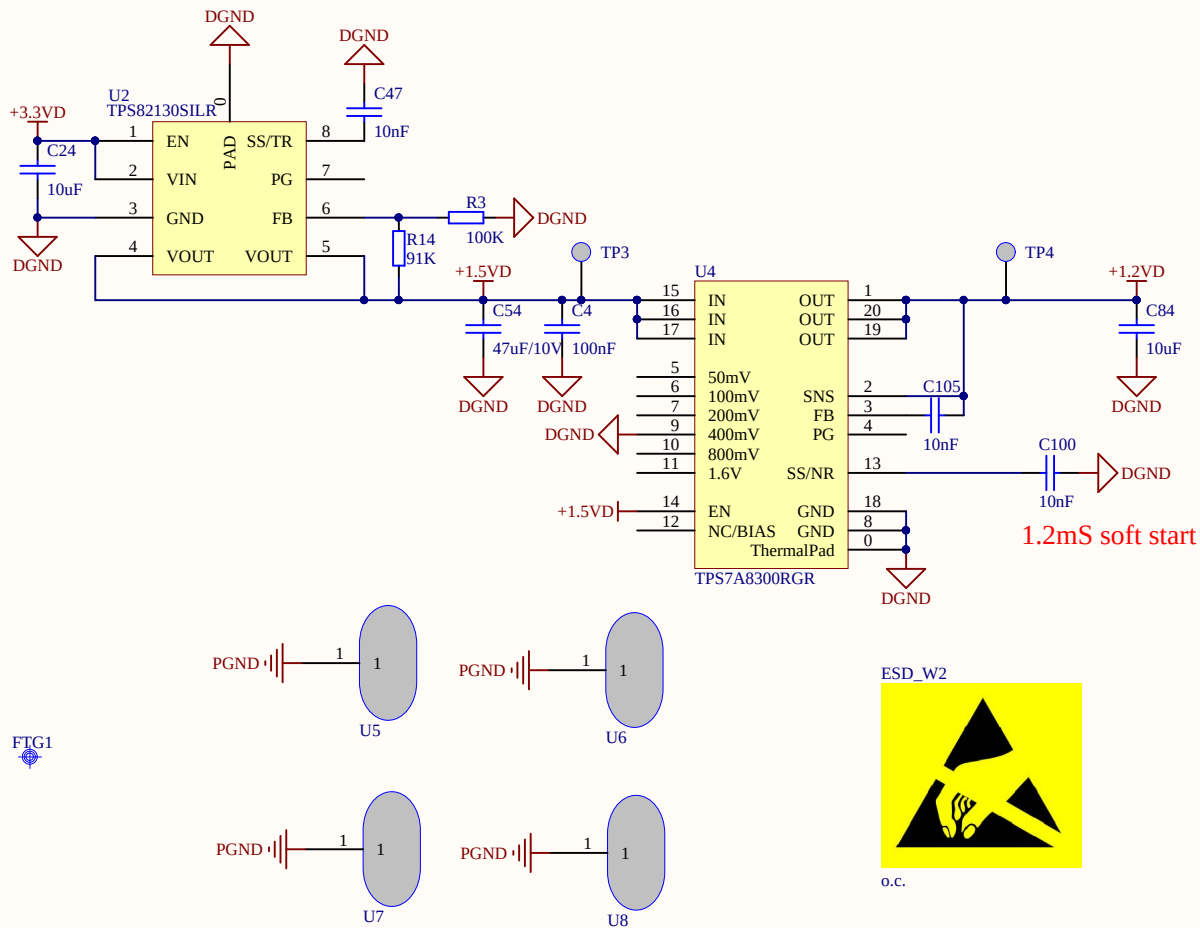
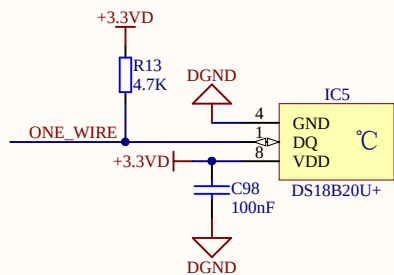
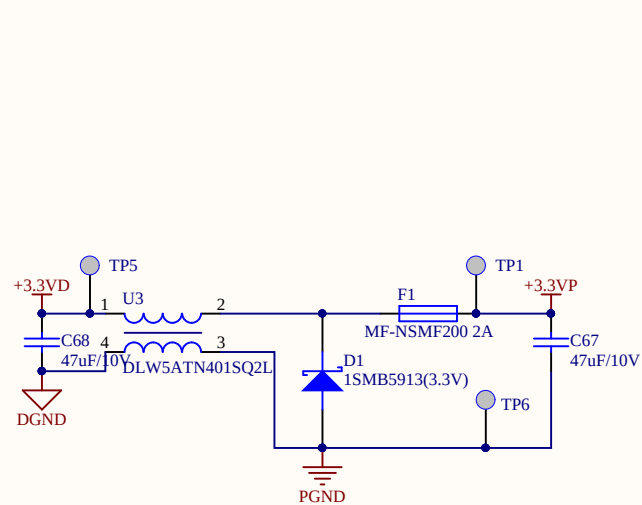
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